Xilinx® Virtex™-5 PCI Express Development Kit

User Guide

AVNET electronics marketing

Table of Contents

Figures

Tables

1.0 Introduction

The purpose of this manual is to describe the functionality and contents of the Virtex-5 LXT/SXT PCI Express Development Kit from Avnet Electronics Marketing. This document includes instructions for operating the board, descriptions of the hardware features and explanations of the test code programmed in the on-board PROM. For reference design documentation, see the PDF file included with the project files of the design.

1.1 Description

The Virtex-5 LXT/SXT PCI Express Development Kit provides a complete hardware environment for designers to accelerate their time to market. The kit delivers a stable platform to develop and test designs targeted to the advanced Xilinx FPGA family. The installed Virtex-5 LXT/SXT device offers a prototyping environment to effectively demonstrate the enhanced benefits of leading edge Xilinx FPGA solutions. Reference designs are included with the kit to exercise standard peripherals on the evaluation board for a quick start to device familiarization.

1.2 Board Features

FPGA

- Xilinx Virtex-5 XC5VLX50T-FF1136 FPGA or
- Xilinx Virtex-5 XC5VLX110T-FF1136 FPGA or
- Xilinx Virtex-5 XC5VSX50T-FF1136 FPGA or
- Xilinx Virtex-5 XC5VSX95T-FF1136 FPGA

I/O Connectors

- Two EXP™ general-purpose I/O expansion connectors
- One 50-pin 0.1” Header supports Avnet SystemACE Module (SAM)

RocketIO™ GTP Transceiver Connectors

- Two Small-Form Pluggable (SFP) cages
- One transceiver supplied on an EXP connector for use by an expansion module
- One Serial ATA signal interface
- One CX4 connector supports 4 lanes @ 3.125 Gbps (only available on LX110T/SX95T boards)
- One PCI Express add-in card interface (8 lanes @ 2.5 Gbps)

Memory

- 64 MB DDR2 SDRAM components
- 256 MB DDR2 SODIMM module (only available on LX110T/SX95T boards)
- 16 MB FLASH

Communication

- RS-232 serial port
- USB 2.0
- Two 10/100/1000 Ethernet ports

Power

- Regulated 3.3V, 2.5V, and 1.2V supply voltages derived from the PCI Express slot or an external 5V supply
- SSTL2 Termination Regulators
- Point of Load Regulators for MGT supply rails

Configuration

- Parallel Flash interface support BPI mode of configuration
- Xilinx Parallel Cable IV or Platform USB Cable support for JTAG Programming/Configuration
- Fly-wire support for Xilinx Parallel Cable III

1.3 Test Files

The Flash on the Virtex-5 LXT/SXT PCI Express Board comes programmed with a PCI Express example design. Additional test files that can be used to verify the functionality of the peripherals on the board can be found on the Avnet Electronics Marketing Design Resource Center (DRC) web site: www.em.avnet.com/drc. The test designs listed below are discussed in Section 3.0.

- PCI Express PIO Example
- Factory Test
- Ethernet Test

1.4 Reference Designs

Reference designs that demonstrate some of the potential applications of the Virtex-5 LXT/SXT PCI Express development board can be downloaded from the Avnet Design Resource Center (www.em.avnet.com/drc). The reference designs include all of the source code and project files necessary to implement the designs. See the PDF document included with each reference design for a complete description of the design and detailed instructions for running a demonstration on the development board. Check the DRC periodically for updates and new designs.

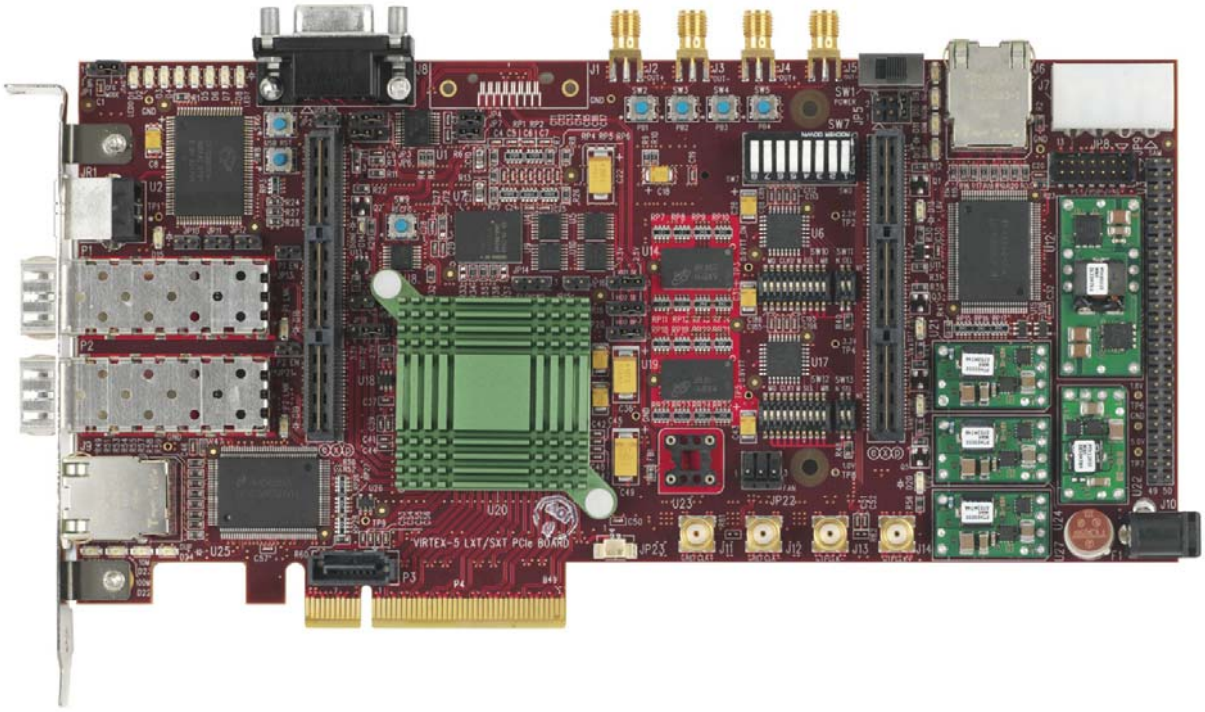


Figure 1 - Virtex-5 LXT/SXT PCI Express Board Picture

1.5 Ordering Information

The following table lists the evaluation kit part numbers and available software options.
Internet link at http://www.em.avnet.com/drc

Part Number	Hardware
AES-XLX-V5LXT-PCIE50-G	Xilinx Virtex-5 PCI Express Kit populated with an XC5VLX50T -1 speed grade device
AES-XLX-V5LXT-PCIE110-G	Xilinx Virtex-5 PCI Express Kit populated with an XC5VLX110T -2 speed grade device
AES-XLX-V5SXT-PCIE50-G	Xilinx Virtex-5 PCI Express Kit populated with an XC5VSX50T -1 speed grade device
AES-XLX-V5SXT-PCIE95-G	Xilinx Virtex-5 PCI Express Kit populated with an XC5VSX95T -2 speed grade device

Table 1 - Ordering Information

2.0 Functional Description

A high-level block diagram of the Virtex-5 LXT/SXT PCI Express board is shown below followed by a brief description of each sub-section.

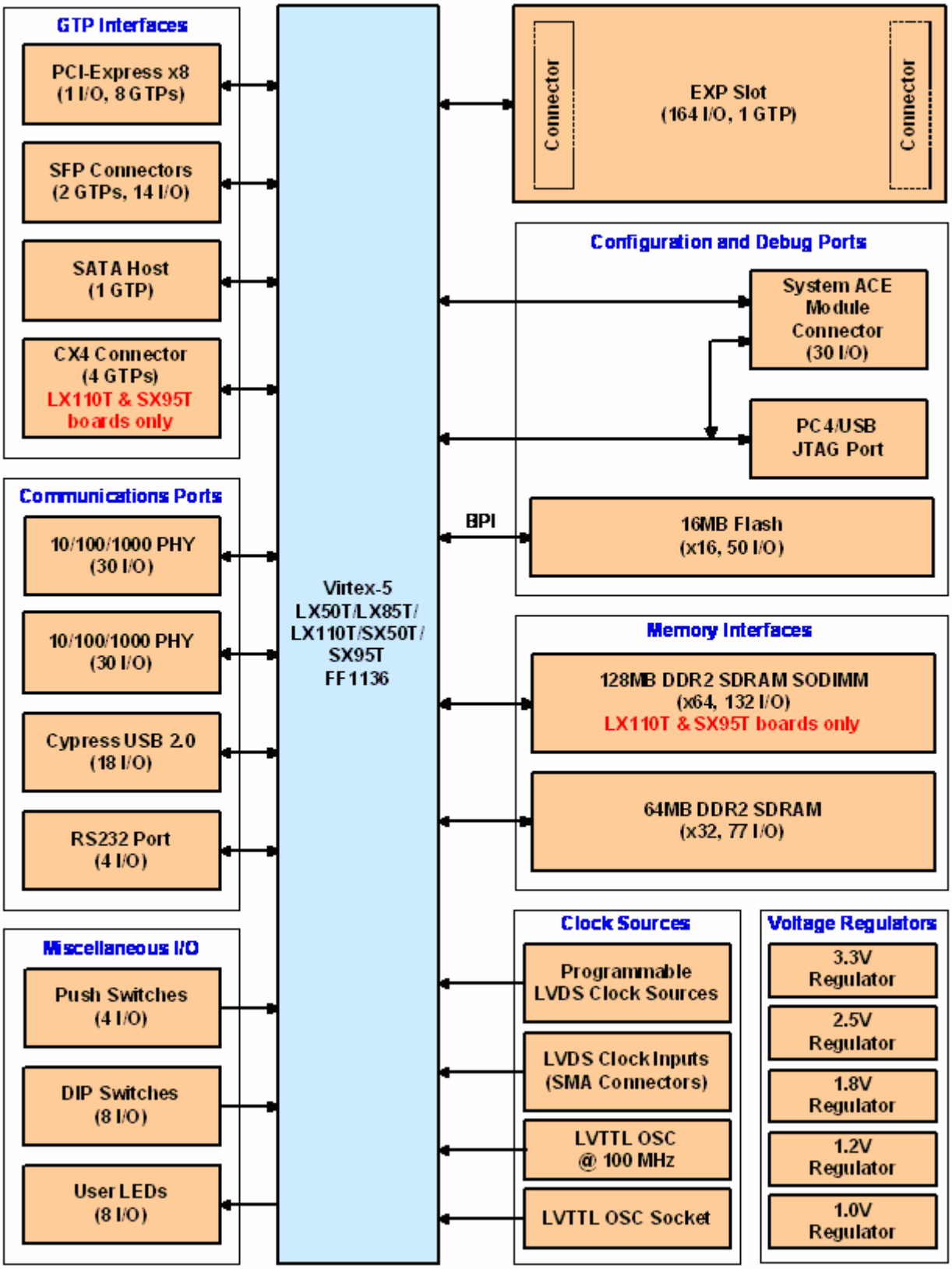


Figure 2 - Virtex-5 LXT/SXT PCI Express Board Block Diagram

2.1 Xilinx Virtex-5 LXT/SXT FPGA

The Virtex-5 LXT/SXT FPGA devices available in the FF1136 package have four embedded Ethernet MAC Blocks, one embedded PCI Express Endpoint Block and six Clock Management Tiles (each tile contains two DCMs and one PLL). The following table shows the differences between these devices.

Device	Number of Slices	BlockRAM (Kb)	DSP48E Slices	GTP Transceivers	I/O Pins
XC5VLX50T	7,200	2,160	48	12	480
XC5VSX50T	8,160	4,752	288	12	480
XC5VLX110T	17,280	5,328	64	16	640
XC5VSX95T	14,720	8,784	640	16	640

Table 2 - Differences between Virtex-5 devices

A common Printed Circuit Board (PCB) is used for all of the FPGA devices. The board was designed to primarily use the I/O pins and transceivers that are common among all of the devices in the FF1136 package. The extra I/O pins available only in the larger devices were used to implement the memory module interface (DDR2 SODIMM). Likewise the extra four transceivers available with the larger devices were used to implement the 10 Gb/s Media Connector interface. Since the smaller devices do not support these extra interfaces, they are not populated on the board.

The Virtex-5 LXT/SXT PCI Express development board uses production silicon devices. The pin-out used for the PCI Express interface supports the Xilinx recommended pin-out for production silicon.

2.2 GTP Interface

The RocketIO™ GTP Transceiver is a full-duplex serial transceiver for point-to-point transmission applications. Up to 24 transceivers are available on a single Virtex-5 LXT/SXT FPGA, depending on the part being used. The transceiver block is designed to operate at any serial bit rate in the range of 100 Mb/s to 3.75 Gb/s per channel, including the specific bit rates used by the communications standards listed in the following table. Multiple channels can be bonded together for increased data throughput. The data width of the FPGA fabric interface is programmable (one or two bytes) allowing the parallel data frequency to be tailored to the user application.

Standards	Channels (# of transceivers)	I/O Bit Rate (Gb/s)
PCI Express	1, 2, 4, 8	2.5
SFI-5	1	2.488 – 3.125
OC-12	1	0.622
OC-48	1	2.488
Fibre Channel	1	1.06
		2.12
Gigabit Ethernet	1	1.25
XAUI (10-Gbit Ethernet)	4	3.125
10-Gbit Fibre Channel	4	3.1875
Infiniband	1, 4	2.5
HD-SDI	1	1.485
		1.4835
Serial ATA	1	1.5
		3.0
Serial Rapid I/O	1, 4	1.25
		2.5
		3.125
Aurora (Xilinx protocol)	1, 2, 3, 4, …	0.100 – 3.75

Table 3 - Communications Standards Supported by the Virtex-5 GTP

The Virtex-5 LXT/SXT transceivers are grouped into tiles with two transceivers per tile. The two transceivers in each tile share a single PLL and other resources involving the reset and power control. A trailing number '0' or '1' is used to distinguish between the two transceivers in the tile. These transceiver tiles are physically located into a single column on the die. Each tile has a placement name associated to its X-Y coordinate on the die. For example, GTP_Dual_X0Y0 is the first tile in the column. The GTP_Dual placement name is used in the User Constraint File (UCF) to map specific tiles on the device to those instantiated in a HDL design. The placement name is different for the devices that support 12 transceivers and the larger devices that support 16 as shown in the following table.

GTP Interface	Lanes	GTP_Dual		Number
		LX50T/SX50T	LX110T/SX95T	
10Gb/s Media Connector	0,1	N/A	GTP_Dual_X0Y7	MGT124
	2,3		GTP_Dual_X0Y0	MGT126
SFP	0,1	GTP_Dual_X0Y5	GTP_Dual_X0Y6	MGT120
Serial ATA	-	GTP_Dual_X0Y4	GTP_Dual_X0Y5	MGT116
EXP	-			
PCI Express	0,1	GTP_Dual_X0Y3	GTP_Dual_X0Y4	MGT112
	2,3	GTP_Dual_X0Y2	GTP_Dual_X0Y3	MGT114
	4,5	GTP_Dual_X0Y1	GTP_Dual_X0Y2	MGT118
	6,7	GTP_Dual_X0Y0	GTP_Dual_X0Y1	MGT122

Table 4 - GTP Placement Names

The following figure shows the 16 RocketIO transceiver ports used on the Virtex-5 LXT/SXT PCI Express board. Print this page and then rotate it right by 90 degrees to see the orientation of the part on the board. The GTP tiles are depicted in their actual locations (rough, not exact).

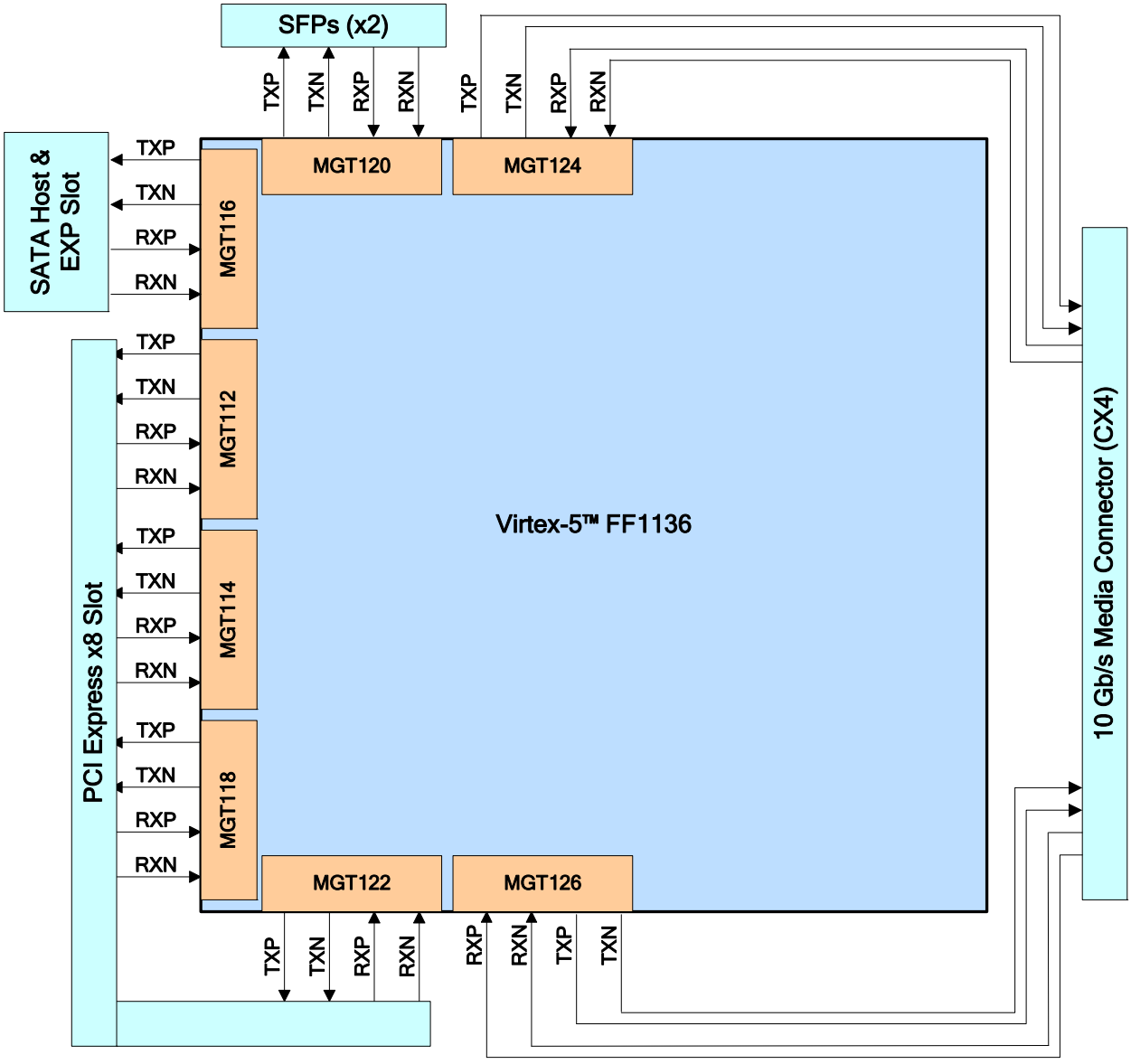


Figure 3 - GTP Ports on the Virtex-5 PCI Express Board

2.2.1 GTP Reference Clock Inputs

Each GTP_Dual tile has a reference clock input that can also be used by adjacent tiles up to 3 tiles away. Several of these reference clock inputs are supplied by on-board clock sources while others are supplied externally. Two programmable LVDS synthesizers are used to provide variable clock sources to the dedicated GTP clock inputs. These synthesizers provide reference clock frequencies that support the full range of line rates. A dedicated pair of differential SMA connectors is connected to one of the GTP clock inputs. The SMA connector inputs are for user clocks generated by external test equipment or by the Virtex-5 itself on one of the SMA output connectors (requires SMA cables to make the connection). PCI Express applications use the 100MHz reference clock provided over the card edge. The following figure shows the clock sources provided to the dedicated GTP clock inputs.

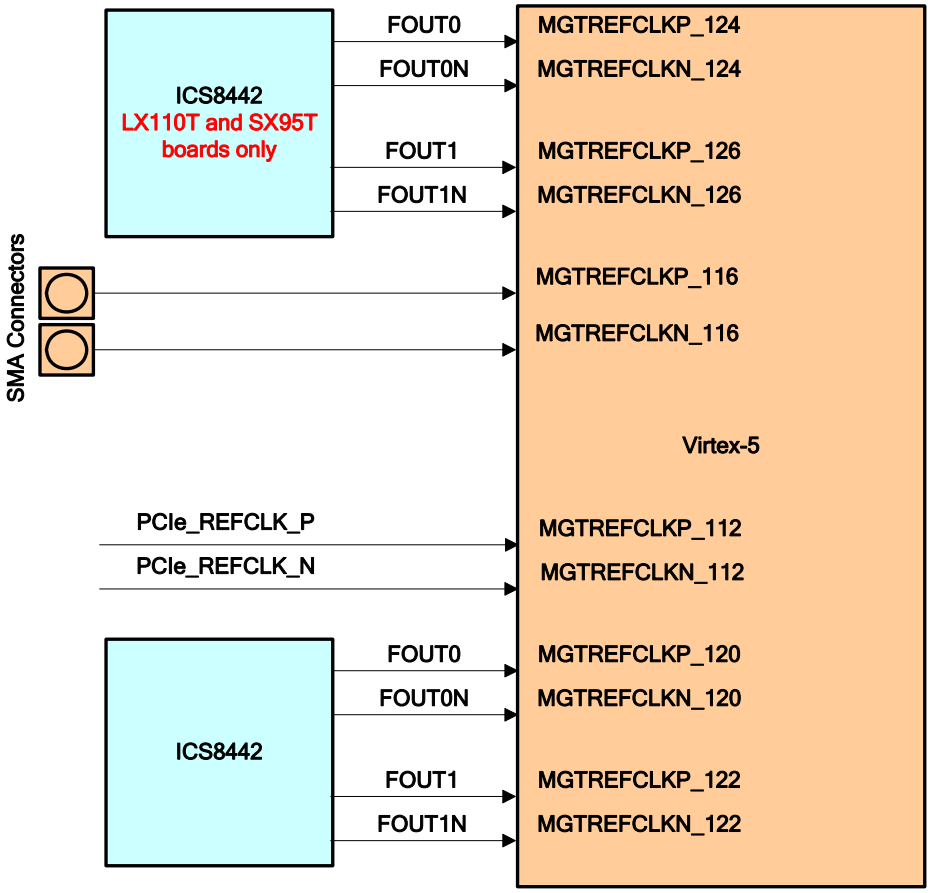


Figure 4 - GTP Clock Sources on the Virtex-5 PCI Express Board

Two sets of differential SMA connectors are connected to regular I/O pins on the Virtex-5 FPGA. These SMA connectors can be used to forward a reference clock out to a scope to provide a trigger input during GTP testing.

2.2.2 PCI Express x8 Add-in Card

Eight of the GTP transceivers are connected to the PCI Express card edge interface. PCI Express is an enhancement to the PCI architecture where the parallel bus has been replaced with a scalable, fully serial interface. The differences in the electrical interface are transparent to the software so existing PCI software implementations are compatible. Use of the Virtex-5 LXT/SXT PCI Express board in a PCI Express application requires the implementation of the PCI Express protocol in the FPGA. The PCI Express Endpoint Block embedded in the Virtex-5 FPGA implements the PCI Express protocol and the physical layer interface to the GTP ports. This block must be instantiated in the user design. For more information, see the "Virtex-5 Endpoint Block for PCI Express Designs User Guide" on the Xilinx web site.

http://direct.xilinx.com/bvdocs/userguides/ug197.pdf.

The PCI Express electrical interface on the Virtex-5 LXT/SXT PCI Express board consists of 8 lanes, each lane having a unidirectional transmit and receive differential pair. Each lane supports the first generation data rate of 2.5 Gbps. In addition to the 8 serial lanes there is a 100MHz reference clock. In order to work in open systems, add-in cards must use the 100MHz reference clock provided over the PCI Express card edge to be frequency locked with the host system. There is also a side band signal from the PCI Express card edge that connects to a regular I/O pin on the Virtex-5 FPGA. The "PERST#" signal is an active low reset signal provided by the host PCI Express slot. The following figure shows the PCI Express interface to the Virtex-5 FPGA.

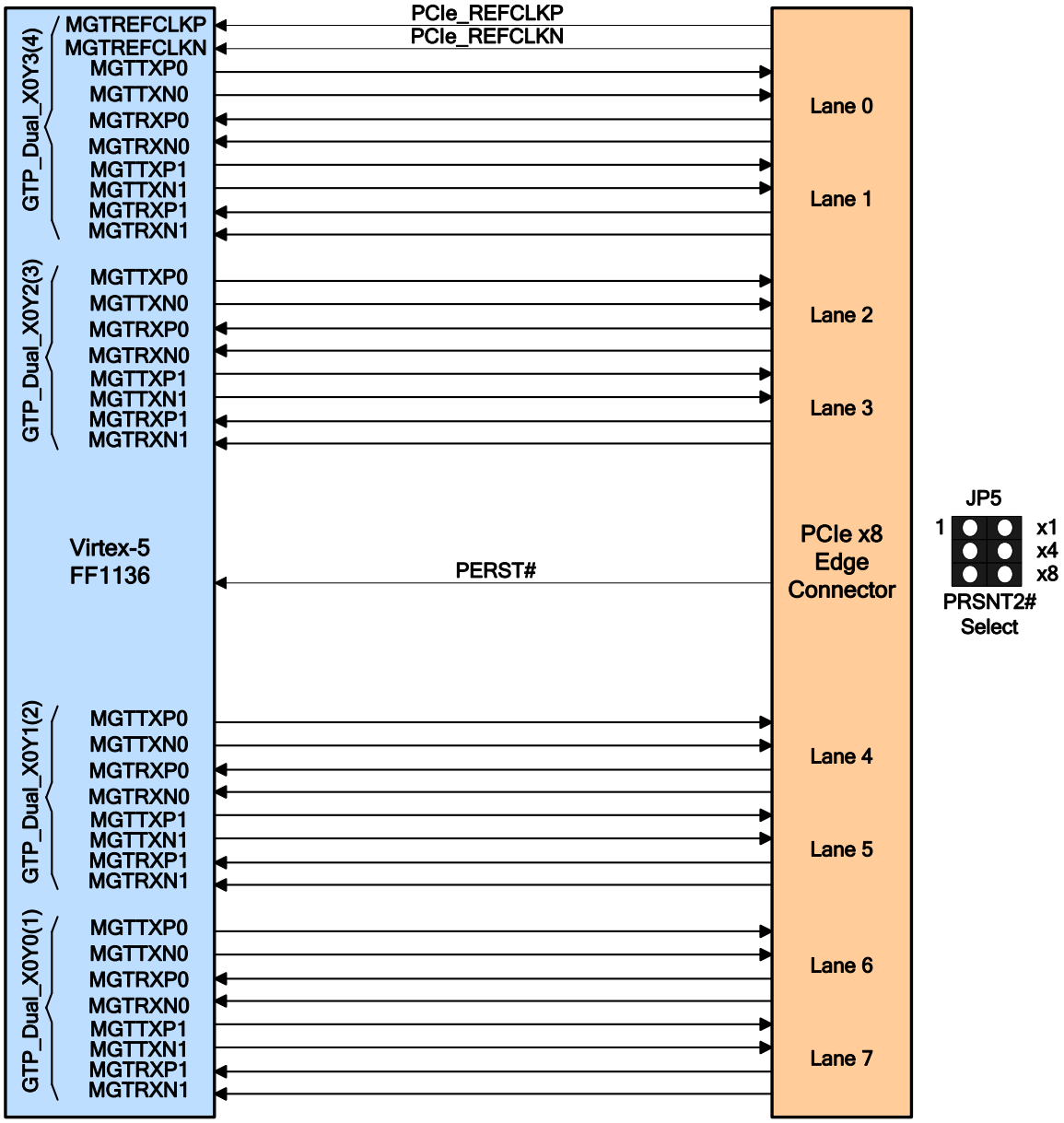


Figure 5 - PCI Express x8 Interface

The lane width of the PCI Express interface is determined by the PRSNT1# and PRSNT2# connections. There are separate PRSNT2# pins for each of the lane options: one lane (x1), four lanes (x4) and eight lanes (X8). These pins are pulled-up on the host motherboard. There is a single PRSNT1# pin that is pulled-low or tied to GND on the host motherboard. The add-in card connects the PRSNT1# pin to the PRSNT2# pin for the widest lane option in most applications, which effectively pulls the corresponding PRSNT2# pin low. This indicates to the host controller the lane width supported by the add-in card. The Virtex-5 LXT/SXT PCI Express board provides the ability for the user to select the lane width by connecting the desired PRSNT2# pin with a jumper on JP5. See Appendix A for more information about the JP5 jumper settings.

The PCI Express transmit lanes are AC coupled (DC blocking capacitors are included in the signal path) on the development board as required by the PCI Express specification. The Virtex-5 LXT/SXT PCI Express board takes advantage of the polarity inversion feature of the GTP transceivers. The "P" and "N" of all of the odd-numbered PCI Express lanes are swapped on the board to improve the PCB routing. Each GTP has attributes that are used to enable polarity inversion on either the transmit or receive pairs, or both. The polarity inversion attributes are "TXPOLARITY" for the transmit pairs and "RXPOLARITY" for the receive pairs. Setting these attributes to a logic 1 enables the inversion.

GTP Instance	Net Name	Connector.pin#	Virtex-5 pin#	P/N Swapped?
LX50T/SX50T: GTP_Dual_X0Y3 LX110T/SX95T: GTP_Dual_X0Y4	PCIe_RX0P	P4.B14	N1	No
	PCIe_RX0N	P4.B15	P1	
	PCIe_TX0P	P4.A16	M2	No
	PCIe_TX0N	P4.A17	N2	
	PCIe_RX1P	P4.B19	R1	Yes (RX)
	PCIe_RX1N	P4.B20	T1	
	PCIe_TX1P	P4.A21	T2	Yes (TX)
	PCIe_TX1N	P4.A22	U2	
LX50T/SX50T: GTP_Dual_X0Y2 LX110T/SX95T: GTP_Dual_X0Y3	PCIe_RX2P	P4.B23	W1	No
	PCIe_RX2N	P4.B24	Y1	
	PCIe_TX2P	P4.A25	V2	No
	PCIe_TX2N	P4.A26	W2	
	PCIe_RX3P	P4.B27	AA1	Yes (RX)
	PCIe_RX3N	P4.B28	AB1	
	PCIe_TX3P	P4.A29	AB2	Yes (TX)
	PCIe_TX3N	P4.A30	AC2	
LX50T/SX50T: GTP_Dual_X0Y1 LX110T/SX95T: GTP_Dual_X0Y2	PCIe_RX4P	P4.B33	AE1	No
	PCIe_RX4N	P4.B34	AF1	
	PCIe_TX4P	P4.A35	AD2	No
	PCIe_TX4N	P4.A36	AE2	
	PCIe_RX5P	P4.B37	AG1	Yes (RX)
	PCIe_RX5N	P4.B38	AH1	
	PCIe_TX5P	P4.A39	AH2	Yes (TX)
	PCIe_TX5N	P4.A40	AJ2	
LX50T/SX50T: GTP_Dual_X0Y0 LX110T/SX95T: GTP_Dual_X0Y1	PCIe_RX6P	P4.B41	AL1	No
	PCIe_RX6N	P4.B42	AM1	
	PCIe_TX6P	P4.A43	AK2	No
	PCIe_TX6N	P4.A44	AL2	
	PCIe_RX7P	P4.B45	AP2	Yes (RX)
	PCIe_RX7N	P4.B46	AP3	
	PCIe_TX7P	P4.A47	AN3	Yes (TX)
	PCIe_TX7N	P4.A48	AN4	

Table 5 - GTP Pin Assignments for PCI Express

2.2.3 SFP Connectors

Two MGT transceivers are connected to Small Form-factor Pluggable (SFP) interfaces, which provide the ability to support optical links with the addition of optical transceiver modules (not included in the kit). The following figure shows a high-level block diagram of the SFP interfaces on the development board. This interface utilizes one GTP_Dual tile and a set of low-speed control signals to interface to two SFP modules. One of the programmable LVDS synthesizers on the board is used to provide the reference clock. The SFP interfaces on the Virtex-5 LXT/SXT PCI Express board have been designed to support transceivers with transmission rates up to 3.75Gbps operating over multimode or single mode fiber.

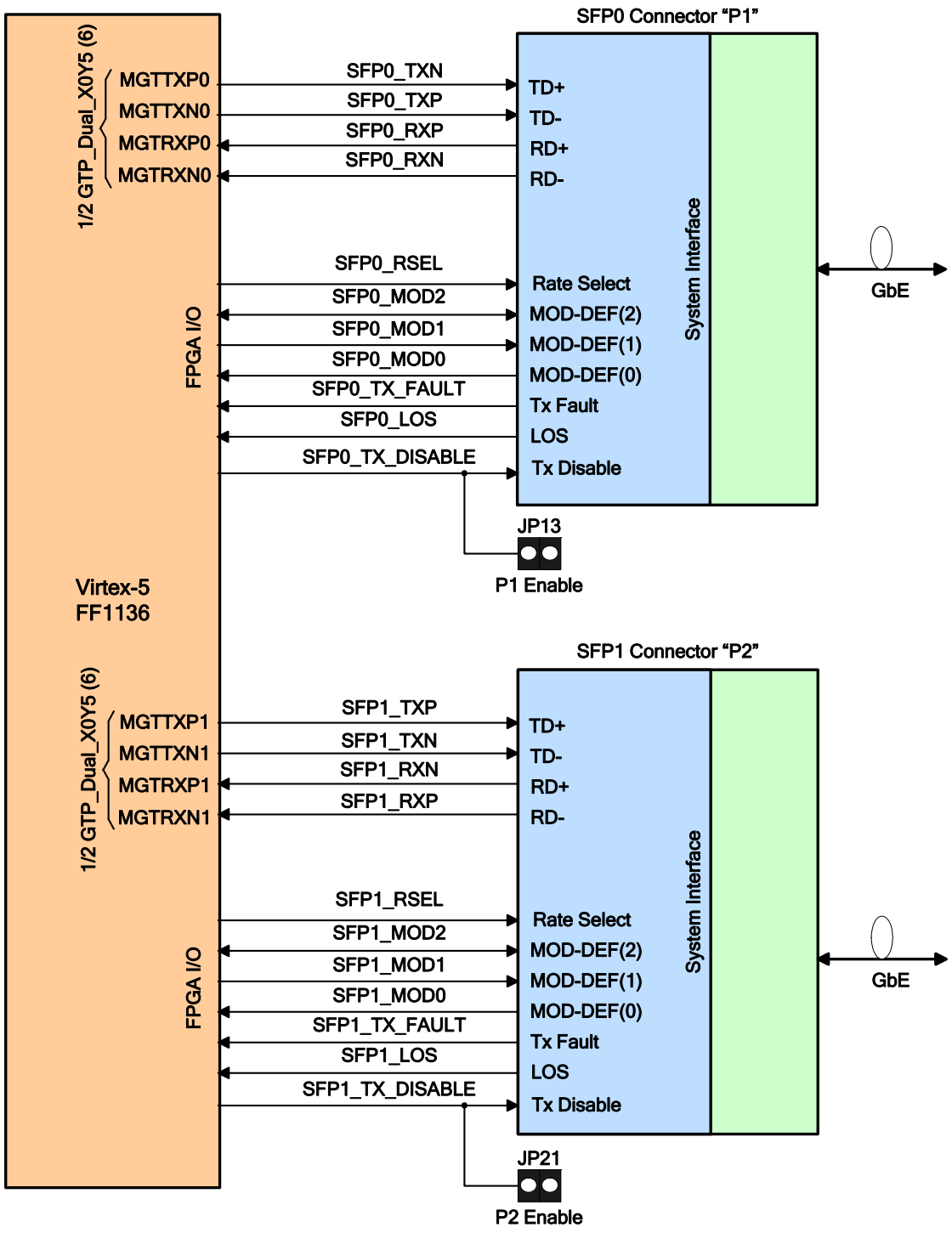


Figure 6 - SFP Module Interfaces

The SFP connectors include a Host Board Connector, and top and bottom EMI cages. The Host Connectors are directly connected or DC coupled to the GTP ports. SFP compliant modules include AC coupling capacitors in the modules for both the transmit and receive signal paths so the AC coupling internal to the Virtex-5 LXT/SXT GTP receiver may be bypassed (RXDCCOUPLE = TRUE). The "P" and "N" of the transmit differential pair is swapped on the board for the SFP0 interface to improve the PCB routing. Set the "TXPOLARITY0" attribute to logic 1 to enable the polarity inversion feature for the transceiver connected to the SFP0 interface. Likewise the receive differential pair is swapped on the board for SFP1. Set the "RXPOLARITY1" attribute to logic 1 to enable polarity inversion for the SFP1 transceiver. MGT120 transceivers 0 and 1 are connected to the two SFP host connectors labeled "P1" and "P2" as indicated in the previous figure. The MGT120 tile is GTP_Dual "X0Y5" in the LX50T/SX50T devices or GTP_Dual "X0Y6" in the LX110T/SX95T devices.

GTP Instance	Net Name	Connector.pin#	Virtex-5 pin#	P/N Swapped?
LX50T/SX50T: GTP_Dual_X0Y5 LX110T/SX95T: GTP_Dual_X0Y6	SFP0_RXN	P1.12	A2	No
	SFP0_RXP	P1.13	A3	
	SFP0_TXP	P1.18	B3	Yes (TX)
	SFP0_TXN	P1.19	B4	
	SFP1_RXN	P2.12	D1	Yes (RX)
	SFP1_RXP	P2.13	C1	
	SFP1_TXP	P2.18	E2	No
	SFP1_TXN	P2.19	D2	

Table 6 - GTP Pin Assignments for the SFP Interfaces

SFP modules connect to the board via the Host Board Connector defined in the SFP Multi-Source Agreement (MSA). This 20-pin connector provides connections for power, ground, high-speed serial data, and the low-speed control signals for controlling the operation of the SFP module. The following figure shows the host connector used on the Virtex-5 LXT/SXT PCI Express board.

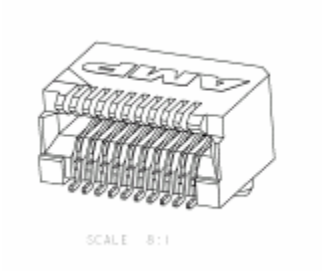


Figure 7 - Host Board Connector AMP 1367073-1 (photo taken from AMP Web Page)

The following table lists the Host Board Connector pin assignments and provides a brief description of each signal.

Pin Number	Name	Function
1	VEET	Transmitter Ground
2	Tx Fault	Transmitter Fault Indication
3	Tx Disable	Transmitter Disable
4	MOD-DEF(2)	Module Definition 2 (Serial Interface Data Line)
5	MOD-DEF(1)	Module Definition 1 (Serial Interface Clock Line)
6	MOD-DEF(0)	Module Definition 0 (Module Present Signals, active low)
7	Rate Select	Not Connected
8	LOS	Loss of Signal
9	VEER	Receiver Ground
10	VEER	Receiver Ground
11	VEER	Receiver Ground
12	RD-	Inverse Received Data Out
13	RD+	Received Data Out
14	VEER	Receiver Ground
15	VCCR	Receiver Power
16	VCCT	Transmitter Power
17	VEET	Transmitter Ground
18	TD+	Transmitter Data In
19	TD-	Inverse Transmitter Data In
20	VEET	Transmitter Ground

Table 7 - SFP Host Connector Pin Description

The following table lists the FPGA I/O assignments for the SFP interfaces.

Net Name	Virtex-5 Pin#
SFP #0	
SFP0_LOS	H29
SFP0_MOD0	E29
SFP0_MOD1	F30
SFP0_MOD2	G30
SFP0_RSEL	F29
SFP0_TX_DISABLE	E31
SFP0_TX_FAULT	F31
SFP #1	
SFP1_LOS	H27
SFP1_MOD0	E26
SFP1_MOD1	G28
SFP1_MOD2	E27
SFP1_RSEL	H28
SFP1_TX_DISABLE	F28
SFP1_TX_FAULT	E28

Table 8 - FPGA I/O Assignments for the SFP Interfaces

2.2.4 Serial ATA Connector

One GTP transceiver is connected to a Serial ATA host connector that can be used to connect an I/O device such as a hard drive to the board. Only the signal connector is present on the Virtex-5 LXT/SXT PCI Express board. Power for the Serial ATA peripheral must be supplied externally. MGT116 transceiver #0 is connected to the vertical cable-to-board connector labeled "P3". The connector is keyed to ensure the correct polarity. The MGT116 tile is GTP_Dual "X0Y4" in the LX50T/SX50T devices or GTP_Dual "X0Y5" in the LX110T/SX95T devices.

GTP Instance	Net Name	Connector.pin#	Virtex-5 pin#	P/N Swapped?
LX50T/SX50T: GTP_Dual_X0Y5	SATA_TXP	P3.2	F2	No
	SATA_TXN	P3.3	G2	
LX110T/SX95T: GTP_Dual_X0Y6	SATA_RXN	P3.5	H1	No
	SATA_RXP	P3.6	G1	

Table 9 - MGT Pin Assignments for Serial ATA

2.2.5 GTP on EXP Connector JX1

One GTP transceiver is brought out to the board-to-board connector labeled "JX1" on the board for use by EXP daughter cards. The MGT116 transceiver #1 is directly connected to JX1 pins 54 and 56 (RX+ and RX-) and pins 53 and 55 (TX+ and TX-). The user must evaluate whether AC coupling is required on the daughter card to safely interface with the Virtex-5 GTP transceiver. The MGT116 tile is GTP_Dual "X0Y4" in the LX50T/SX50T devices or GTP_Dual "X0Y5" in the LX110T/SX95T devices.

GTP Instance	Net Name	Connector.pin#	Virtex-5 pin#	P/N Swapped?
LX50T/SX50T: GTP_Dual_X0Y5	EXP_TXP	JX1.53	L2	No
	EXP_TXN	JX1.55	K2	
LX110T/SX95T: GTP_Dual_X0Y6	EXP_RXP	JX1.54	K1	No
	EXP_RXN	JX1.56	J1	

Table 10 - MGT Pin Assignments for SMA Connectors

2.2.6 10 Gb/s Media Connector

Four GTP transceivers are connected to a board-to-cable connector for general purpose use. The connector footprint on the Virtex-5 LXT/SXT PCI Express board supports the jack screw attachment version of the Molex LaneLink™ 4X I/O connector. This surface-mount connector is optimized for high-speed differential signals supporting serial data rates up to 3.125 Gb/s. This interface can be used for short-range, point-to-point applications requiring full-duplex operation over four lanes (8 unidirectional signals: 4 transmit pairs and 4 receive pairs). This interface utilizes two GTP tiles to support four RocketIO transceivers running at 3.125 Gb/s to implement a 10 Gb/s channel. A single cable can be used to connect to EXP daughter cards with 10 Gb/s capable PHY devices for prototyping purposes. The cable is not included in the kit but can be purchased from an authorized Molex distributor (P/N: 74506-3001). The LaneLink 4X connector is labeled "J1" on the board. The following figure shows a high-level block diagram of the 10 Gb/s interface on the development board.

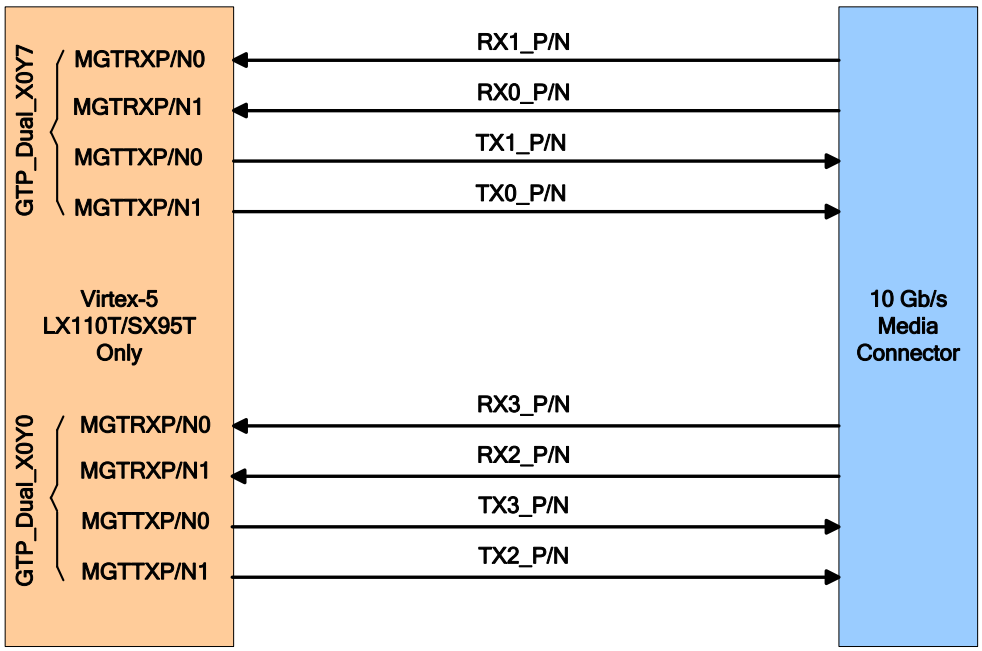


Figure 8 - 10 Gb/s Media Connector Interface

The 10 Gb/s Media Connector is directly connected or DC coupled to the GTP ports. Care must be taken not to exceed the GTP receiver tolerances when interfacing to external devices. The AC coupling internal to the Virtex-5 LXT/SXT MGT receiver should not be bypassed unless the external connection has DC blocking capacitors on the transmit lanes. The "P" and "N" of some of the differential pairs are swapped on the board to improve the PCB routing to the 10 Gb/s Media Connector. Set the "RXPOLARITYx" and "TXPOLARITYx" attributes to logic 1 to enable the polarity inversion feature for the transceivers indicated in the following table (see the "P/N Swapped" column). This interface utilizes four of the GTP ports; MGT124 transceivers 0 and 1, and MGT126 transceivers 0 and 1. The programmable LVDS clock synthesizer labeled "U17" on the board is used to provide the reference clock to both tiles.

GTP Instance	Net Name	Connector.pin#	Virtex-5 pin#	P/N Swapped?
LX110T/SX95T: GTP_Dual_X0Y7	CX4_RX0P	J1.2	A6	No
	CX4_RX0N	J1.3	A7	
	CX4_TX0N	J1.23	B6	No
	CX4_TX0P	J1.24	B5	
	CX4_RX1P	J1.5	A8	Yes (RX)
	CX4_RX1N	J1.6	A9	
	CX4_TX1N	J1.20	B10	Yes (TX)
	CX4_TX1P	J1.21	B9	
LX110T/SX95T: GTP_Dual_X0Y0	CX4_RX2P	J1.8	AP9	No
	CX4_RX2N	J1.9	AP8	
	CX4_TX2N	J1.17	AN10	Yes (TX)
	CX4_TX2P	J1.18	AN9	
	CX4_RX3P	J1.11	AP6	No
	CX4_RX3N	J1.12	AP7	
	CX4_TX3N	J1.14	AN6	No
	CX4_TX3P	J1.15	AN5	

Table 11 - GTP Pin Assignments for 10Gbps Media Connector

2.3 Memory

The Virtex-5 LXT/SXT PCI Express development board is populated with both high-speed RAM and non-volatile ROM to support various types of applications. The boards with the LX50T/SX50T devices have 64 Megabytes (MB) of DDR2 SDRAM and 16 MB of Flash. The boards with the LX110T/SX95T devices also have 64MB of DDR2 SDRAM but have a larger density Flash device (32MB) and an additional 256MB memory module. The memory module interface is only available with the larger FPGAs that have the extra four I/O banks. The I/O pins used for the module interface are no-connects in the smaller devices. If additional memory is necessary for development, check the Avnet Design Resource Center (DRC) for the availability of EXP compliant daughter cards with expansion memory (sold separately). Here is the link to the DRC web page: www.em.avnet.com/drc.

2.3.1 DDR2 SDRAM Interface

Two Micron DDR2 SDRAM devices, part number MT47H16M16BG-5E, make up the 32-bit data bus. Each device provides 32MB of memory on a single IC and is organized as 4 Megabits x 16 x 4 banks (256 Megabit). The Virtex-5 LXT/SXT PCI Express Board can support larger devices with addressing support for up to 128MB (two 512-Megabit devices). The device has an operating voltage of 1.8V and the interface is JEDEC Standard SSTL_18 (Class I for unidirectional signals, Class II for bidirectional signals). The -5 speed grade supports 5 ns cycle times with a 3 clock read latency (DDR2-400). The following figure shows a high-level block diagram of the DDR2 SDRAM interface on the development board.

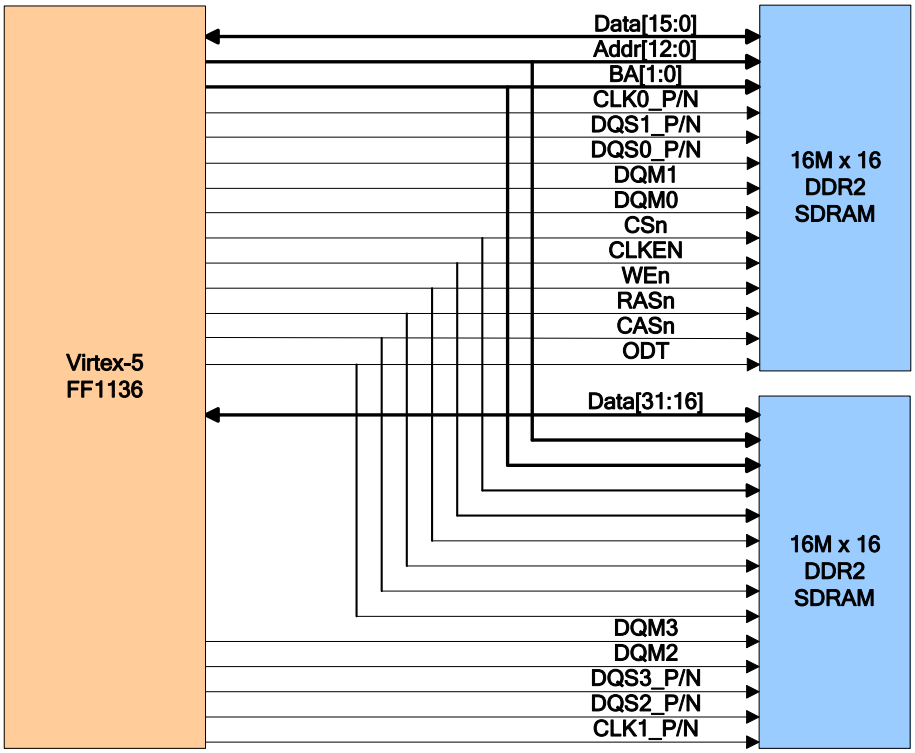


Figure 9 - DDR2 SDRAM Interface

The DDR2 signals are connected to I/O Banks 17 and 21 of the Virtex-5 LXT/SXT FPGA. The output supply pins (VCCO) for Banks 17 and 21 are connected to 1.8 Volts. This supply rail can be measured at test point TP6, which can be found in the area between the power modules and the SAM header labeled “JP9”. The reference voltage pins (VREF) for Banks 17 and 21 are connected to the reference output of the National LP2997 DDR2 Termination Linear Regulator. This rail provides the voltage reference necessary for the SSTL_18 I/O standard. The LP2997 regulator also provides the termination supply rail. The termination voltage is 0.9 Volts and can be measured at test point TP5, which can be found next to the DDR2 SDRAM device labeled “U19”.

The following table provides timing and other information about the Micron device necessary to implement a DDR2 memory controller.

MT47H16M16BG-5E: Timing Parameters	Time (ps) or Number
Load Mode Register time (TMRD)	2 tCK
Write Recovery time (TWR)	15000
Write-to-Read Command Delay (TWTR)	10000
Delay between ACT and PRE Commands (TRAS)	40000
Delay after ACT before another ACT (TRC)	55000
Delay after AUTOREFRESH Command (TRFC)	75000
Delay after ACT before READ/WRITE (TRCD)	15000
Delay after ACT before another row ACT (TRRD)	10000
Delay after PRECHARGE Command (TRP)	15000
Refresh Command Interval (TREFC)	70000000
Avg. Refresh Period (TREFI)	7800000
Memory Data Width (DWIDTH) (2 devices)	32
Row Address Width (AWIDTH)	13
Column Address Width (COL_AWIDTH)	9
Bank Address Width (BANK_AWIDTH)	2
Memory Range (64 MB total)	0x3FFFFFF

Table 12 - DDR2 SDRAM Timing Parameters

The following guidelines were used in the design of the DDR2 interface to the Virtex-5 LXT/SXT FPGA. These guidelines are based on Micron recommendations and board level simulation.

- 50 ohm* controlled trace impedance
- Dedicated data bus with matched trace lengths (+/- 50 mils)
- Memory clocks and data strobes routed differentially
- Series termination on bidirectional signals at the memory device
- Parallel termination following the memory device connection on shared signals (control, address)
- 50 ohm* pull-up resistor to the termination supply (0.9V) on clock signals
- 100 ohm* pull-up resistor to the termination supply on each branch of shared signals (control, address)
- Termination supply that can both source and sink current
- Feedback clock routed with twice the length to simulate the total flight time

* Ideal impedance values. Actual may vary.

Some of the design considerations were specific to the Virtex-5 architecture. For example, the data strobe signals (DQS) were placed on Clock Capable I/O pins in order to support data capture techniques utilizing the SERDES function of the Virtex-5 I/O blocks. The appropriate DDR2 memory signals were placed in the clock regions that correspond to these particular Clock Capable I/O pins.

The following table contains the FPGA pin numbers for the DDR2 SDRAM interface.

Net Name	Virtex-5 pin#		Net Name	Virtex-5 pin#
DDR2_A0	V27		DDR2_D0	AF29
DDR2_A1	V28		DDR2_D1	AF31
DDR2_A2	W24		DDR2_D2	Y29
DDR2_A3	AH28		DDR2_D3	AJ31
DDR2_A4	Y26		DDR2_D4	AK31
DDR2_A5	AG28		DDR2_D5	Y28
DDR2_A6	W27		DDR2_D6	AE31
DDR2_A7	AF28		DDR2_D7	AC29
DDR2_A8	AA28		DDR2_D8	AD31
DDR2_A9	AE28		DDR2_D9	AH29
DDR2_A10	W29		DDR2_D10	AA30
DDR2_A11	Y27		DDR2_D11	AJ30
DDR2_A12	AE27		DDR2_D12	AH30
			DDR2_D13	AA29
DDR2_BA0	AC27		DDR2_D14	AG30
DDR2_BA1	AC28		DDR2_D15	Y31
			DDR2_D16	AE26
DDR2_CS#	W25		DDR2_D17	AG25
DDR2_ODT	V25		DDR2_D18	AJ25
DDR2_WE#	AB28		DDR2_D20	AA26
DDR2_RAS#	W26		DDR2_D21	AH25
DDR2_CAS#	V24		DDR2_D22	AF25
DDR2_CLKEN	AB27		DDR2_D23	AF26
DDR2_CK0	AE29		DDR2_D24	AJ27
DDR2_CK0#	AD29		DDR2_D25	AC25
DDR2_CK1	AD26		DDR2_D26	AJ26
DDR2_CK1#	AD25		DDR2_D27	AF24
			DDR2_D28	AE24
DDR2_DQS0	AB31		DDR2_D29	AK26
DDR2_DQS0#	AA31		DDR2_D30	AC24
DDR2_DQS1	AB30		DDR2_D31	AH27
DDR2_DQS1#	AC30			
DDR2_DQS2	AK29		DDR2_DM0	AF30
DDR2_DQS2#	AJ29		DDR2_DM1	AD30
DDR2_DQS3	AK28		DDR2_DM2	AA25
DDR2_DQS3#	AK27		DDR2_DM3	AA24
DDR2_CLK_FB_OUT	AD24			
DDR2_CLK_FB_IN	AG18			

Table 13 - FPGA Pin Assignments for DDR2 SDRAM

2.3.2 DDR2 SODIMM Interface (LX110T/SX95T Only)

The extra I/O pins available with the LX110T and SX95T devices are used to implement a 200-pin, small outline, dual in-line memory module (SODIMM) interface. A Micron DDR2 SDRAM module, part number MT4HTF3264HY-53ED3, is populated in the SODIMM connector labeled “U33” on the backside of the Virtex-5 LXT/SXT PCI Express board. This single rank module provides 256MB of memory organized as 32 Meg x 64. The bandwidth of the -53E speed grade module is 4.3GB/s with a memory clock of 533MHz (3.75ns). The Virtex-5 LXT/SXT PCI Express board was designed to support larger density modules with eight-bank addressing and dual rank modules with two chip selects.

The DDR2 SODIMM signals are connected to I/O Banks 5, 6, 23 and 25 of the Virtex-5 LXT/SXT FPGA. The output supply pins (VCCO) for these banks are connected to 1.8 Volts. A second National LP2997 Termination Regulator is dedicated to the SODIMM interface to provide the reference and termination voltage rails (0.9 Volts) necessary to implement the SSTL_18 I/O standard. The termination voltage rail “0.9VTT_DM” can be measured at test point TP3, which can be found next to the DDR2 SDRAM device labeled “U14”.

The following table provides timing and other information about the Micron device necessary to implement a DDR2 SODIMM memory controller.

MT4HTF3264HY-53ED3: Timing Parameters	Time (ps) or Number
Load Mode Register time (TMRD)	2 tCK
Write Recovery time (TWR)	15000
Write-to-Read Command Delay (TWTR)	10000
Delay between ACT and PRE Commands (TRAS)	40000
Delay after ACT before another ACT (TRC)	55000
Delay after AUTOREFRESH Command (TRFC)	75000
Delay after ACT before READ/WRITE (TRCD)	15000
Delay after ACT before another row ACT (TRRD)	10000
Delay after PRECHARGE Command (TRP)	15000
Refresh Command Interval (TREFC)	70000000
Avg. Refresh Period (TREFI)	7800000
Memory Data Width (DWIDTH)	64
Row Address Width (AWIDTH)	13
Column Address Width (COL_AWIDTH)	10
Bank Address Width (BANK_AWIDTH)	2
Memory Range (256 MB total)	0xFFFFFFF

Table 14 - DDR2 SODIMM Parameters

The following guidelines were used in the design of the DDR2 SODIMM interface to the Virtex-5 LXT/SXT FPGA. These guidelines are based on Micron recommendations and board level simulation.

- 50 ohm* controlled trace impedance
- Dedicated data bus with matched trace lengths (+/- 50 mils)
- Memory clocks and data strobes routed differentially
- 50 ohm* pull-up resistor to the termination supply (0.9V) on clock, control and address signals
- Termination supply that can both source and sink current
- Feedback clock routed with twice the length to simulate the total flight time

* Ideal impedance values. Actual may vary.

Some of the design considerations were specific to the Virtex-5 architecture. For example, the data strobe signals (DQS) were placed on Clock Capable I/O pins in order to support data capture techniques utilizing the SERDES function of the Virtex-5 I/O blocks. The appropriate DDR2 memory signals were placed in the clock regions that correspond to these particular Clock Capable I/O pins.

The following table contains the FPGA pin numbers for the DDR2 SODIMM interface.

Net Name	Virtex-5 pin#	Net Name	Virtex-5 pin#	Net Name	Virtex-5 pin#
DDR2_DIMM_A0	D29	DDR2_DIMM_D0	AJ12	DDR2_DIMM_D32	C22
DDR2_DIMM_A1	D26	DDR2_DIMM_D1	AK12	DDR2_DIMM_D33	A21
DDR2_DIMM_A2	D27	DDR2_DIMM_D2	AJ14	DDR2_DIMM_D34	C20
DDR2_DIMM_A3	C27	DDR2_DIMM_D3	AK14	DDR2_DIMM_D35	B20
DDR2_DIMM_A4	AL31	DDR2_DIMM_D4	AK13	DDR2_DIMM_D36	D25
DDR2_DIMM_A5	AP26	DDR2_DIMM_D5	AL13	DDR2_DIMM_D37	A25
DDR2_DIMM_A6	AM31	DDR2_DIMM_D6	AN15	DDR2_DIMM_D38	A24
DDR2_DIMM_A7	AP31	DDR2_DIMM_D7	AP15	DDR2_DIMM_D39	C23
DDR2_DIMM_A8	AP25	DDR2_DIMM_DM0	AL14	DDR2_DIMM_DM4	C24
DDR2_DIMM_A9	AH24	DDR2_DIMM_DQS0	AK16	DDR2_DIMM_DQS4	B25
DDR2_DIMM_A10	E24	DDR2_DIMM_DQS0#	AL16	DDR2_DIMM_DQS4#	C25
DDR2_DIMM_A11	AL30				
DDR2_DIMM_A12	AN24	DDR2_DIMM_D8	AL15	DDR2_DIMM_D40	A20
		DDR2_DIMM_D9	AM15	DDR2_DIMM_D41	C19
DDR2_DIMM_BA0	D24	DDR2_DIMM_D10	AJ17	DDR2_DIMM_D42	C18
DDR2_DIMM_BA1	C28	DDR2_DIMM_D11	AK17	DDR2_DIMM_D43	B18
DDR2_DIMM_BA2	D31	DDR2_DIMM_D12	AM16	DDR2_DIMM_D44	A23
		DDR2_DIMM_D13	AP16	DDR2_DIMM_D45	B23
DDR2_DIMM_S0#	F24	DDR2_DIMM_D14	AN17	DDR2_DIMM_D46	B22
DDR2_DIMM_S1#	AP24	DDR2_DIMM_D15	AP17	DDR2_DIMM_D47	B21
DDR2_DIMM_ODT0	E21	DDR2_DIMM_DM1	AM17	DDR2_DIMM_DM5	A19
DDR2_DIMM_ODT1	AH23	DDR2_DIMM_DQS1	AJ16	DDR2_DIMM_DQS5	B27
DDR2_DIMM_WE#	E23	DDR2_DIMM_DQS1#	AJ15	DDR2_DIMM_DQS5#	A26
DDR2_DIMM_RAS#	C30				
DDR2_DIMM_CAS#	E22	DDR2_DIMM_D16	AN20	DDR2_DIMM_D48	E18
DDR2_DIMM_CKE0	D22	DDR2_DIMM_D17	AM20	DDR2_DIMM_D49	F18
DDR2_DIMM_CKE1	AM30	DDR2_DIMM_D18	AP20	DDR2_DIMM_D50	G17
DDR2_DIMM_CK0	AN19	DDR2_DIMM_D19	AM21	DDR2_DIMM_D51	D17
DDR2_DIMM_CK0#	AP19	DDR2_DIMM_D20	AM27	DDR2_DIMM_D52	D20
DDR2_DIMM_CK1	A30	DDR2_DIMM_D21	AN27	DDR2_DIMM_D53	F20
DDR2_DIMM_CK1#	B30	DDR2_DIMM_D22	AM28	DDR2_DIMM_D54	D19
		DDR2_DIMM_D23	AN28	DDR2_DIMM_D55	E19
DDR2_DIMM_SA0	B15	DDR2_DIMM_DM2	AP27	DDR2_DIMM_DM6	G20
DDR2_DIMM_SA1	A15	DDR2_DIMM_DQS2	AN25	DDR2_DIMM_DQS6	E17
		DDR2_DIMM_DQS2#	AM25	DDR2_DIMM_DQS6#	E16
DDR2_DIMM_SDA	D15				
DDR2_DIMM_SCL	F15	DDR2_DIMM_D24	AP21	DDR2_DIMM_D56	F16
		DDR2_DIMM_D25	AP22	DDR2_DIMM_D57	D16
DDR2_DIMM_EVENT	D21	DDR2_DIMM_D26	AM22	DDR2_DIMM_D58	C14
		DDR2_DIMM_D27	AN23	DDR2_DIMM_D59	F14
DDR2_CLK_FB_OUT	D30	DDR2_DIMM_D28	AL29	DDR2_DIMM_D60	B17
DDR2_CLK_FB_IN	J16	DDR2_DIMM_D29	AN29	DDR2_DIMM_D61	C17
		DDR2_DIMM_D30	AN30	DDR2_DIMM_D62	B16
		DDR2_DIMM_D31	AP30	DDR2_DIMM_D63	A16
		DDR2_DIMM_DM3	AN22	DDR2_DIMM_DM7	A14
		DDR2_DIMM_DQS3	AL25	DDR2_DIMM_DQS7	D14
		DDR2_DIMM_DQS3#	AL24	DDR2_DIMM_DQS7#	E14

Table 15 - FPGA Pin Assignments for DDR2 SODIMM

2.3.3 Flash Interface

The Flash memory consists of a single Intel StrataFlash Embedded Memory (P30) device in a 64-ball Easy BGA package. The boards with the LX50T/SX50T FPGA have a 128-Mbit Flash device while the boards with the larger LX110T/SX95T FPGA have a 256-Mbit Flash. The P30 device is an asynchronous memory that also supports a synchronous-burst read mode for high-performance applications. The P30 device has an 85 nanosecond access time. The footprint on the Virtex-5 LXT/SXT PCI Express board also supports the J3 device (28FxxxJ3A) in the same package with a jumper resistor to select the appropriate VCC voltage (1.8V for the P30 device or 3.3V for the J3 device). The jumper resistor labeled "JT2" on the board sets the supply voltage (1.8V default). The Flash interface connects to the designated pins required for BPI configuration mode. These pins are in Banks 1, 2 and 4 of the Virtex-5 FPGA. The Flash I/O voltage (VCCQ) is set to 3.3V to match the VCCO voltage of Banks 1 and 2. The following figure shows a high-level block diagram of the Flash interface on the development board.

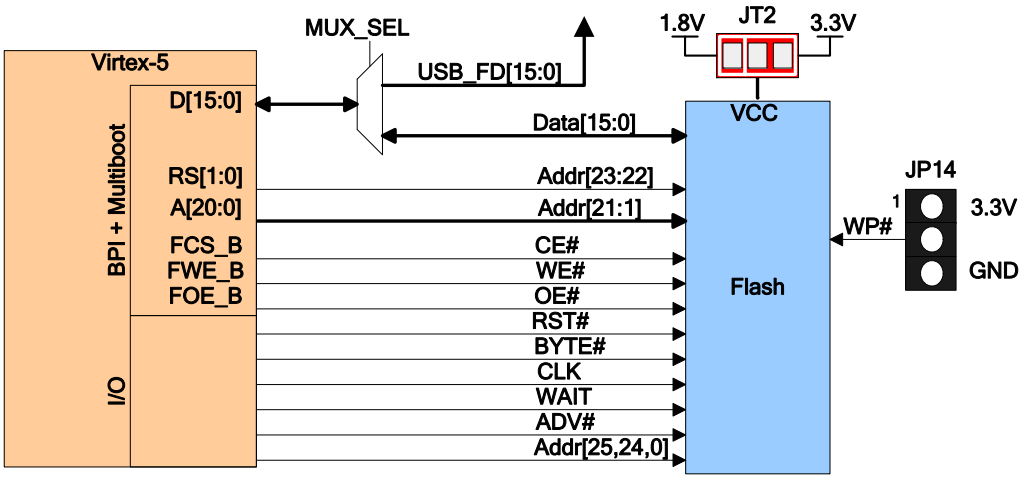


Figure 10 - Flash Interface

The following table contains the FPGA pin numbers for the Flash interface.

Net Name	Virtex-5 pin#		Net Name	Virtex-5 pin#
FLASH_A0	AG12		FLASH_D0	AD19
FLASH_A1	K12		FLASH_D1	AE19
FLASH_A2	K13		FLASH_D2	AE17
FLASH_A3	H23		FLASH_D3	AF16
FLASH_A4	G23		FLASH_D4	AD20
FLASH_A5	H12		FLASH_D5	AE21
FLASH_A6	J12		FLASH_D6	AE16
FLASH_A7	K22		FLASH_D7	AF15
FLASH_A8	K23		FLASH_D8	AH13
FLASH_A9	K14		FLASH_D9	AH14
FLASH_A10	L14		FLASH_D10	AH19
FLASH_A11	H22		FLASH_D11	AH20
FLASH_A12	G22		FLASH_D12	AG13
FLASH_A13	J15		FLASH_D13	AH12
FLASH_A14	K16		FLASH_D14	AH22
FLASH_A15	K21		FLASH_D15	AG22
FLASH_A16	J22			
FLASH_A17	L16		FLASH_CE#	AE14
FLASH_A18	L15		FLASH_WE#	AF20
FLASH_A19	L20		FLASH_OE#	AF14
FLASH_A20	L21		FLASH_RST#	T24
FLASH_A21	AE23		FLASH_BYTE#	AF21
FLASH_A22	AE12		FLASH_WAIT	P25
FLASH_A23	AE13		FLASH_ADV#	N25
FLASH_A24	AE22		FLASH_CLK	R24
FLASH_A25	AF23			

Table 16 - Flash Interface Pin Assignments

2.4 Clock Sources

The Virtex-5 LXT/SXT PCI Express board includes all of the necessary clocks on the board to implement high-speed logic and RocketIO transceiver designs as well as providing the flexibility for the user to supply their own application specific clocks. The clock sources described in this section are used to derive the required clocks for the memory and communications devices, and the general system clocks for the logic design. This section also provides information on how to supply external user clocks to the FPGA via the on-board connectors and oscillator socket. For a description of the GTP reference clock sources, see Section 2.2.1.

The following figure shows the clock nets connected to the I/O banks containing the global clock input pins on the Virtex-5 LXT/SXT FPGA. Sixteen out of the twenty global clock inputs of the Virtex-5 FPGA are utilized on the board. However the majority of these inputs are for expansion clocks and user inputs. It should be noted that single-ended clock inputs must be connected to the P-side of the pin pair because a direct connection to the global clock tree only exists on this pin. The I/O voltages (VCCO) for the two FPGA banks containing the global clock input pins (Banks 3 and 4) are jumper selectable to either 2.5V or 3.3V. In order to use the differential clock inputs as LVDS inputs, the VCCO voltage for the corresponding bank must be set for 2.5V since the Virtex-5 FPGA does not support 3.3V differential signaling. Single-ended clock inputs do not have this restriction and may be either 2.5V or 3.3V. The interface clocks coming from 3.3V devices on the board are level-shifted to the appropriate VCCO voltage by CB3T standard logic devices prior to the Virtex-5 input pins. Setting both of the voltage selection jumpers to 2.5V (default condition) enables the board to support both single-ended and differential clock inputs.

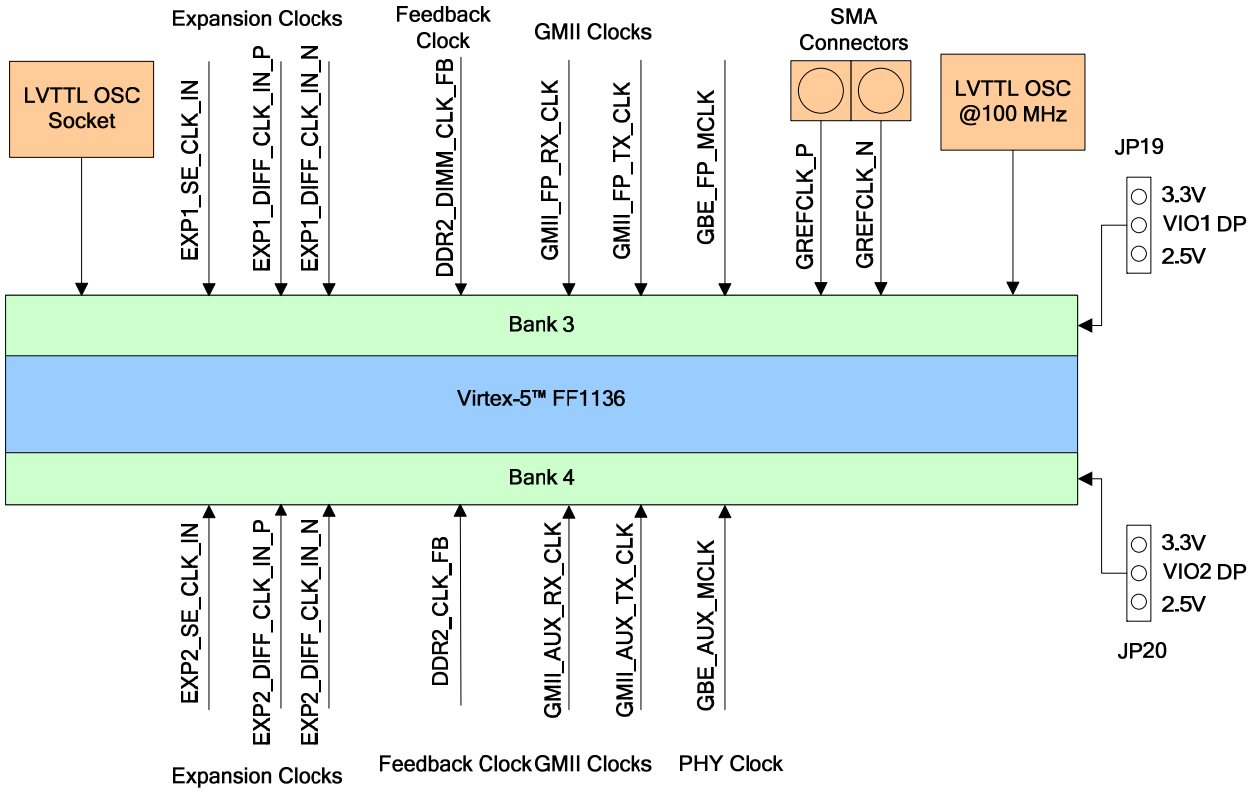


Figure 11 - Clock Nets Connected to Global Clock Inputs

The on-board 100MHz oscillator provides the system clock input to the global clock tree. This single-ended, 100MHz clock can be used in conjunction with the Virtex-5 Clock Management Tiles (CMTs) to generate the various logic clocks and the clocks forwarded to the DDR2 SDRAM devices. The interface clocks supplied by the communications devices are derived from dedicated crystal oscillators.

Reference#	Frequency	Derived Interface Clock	Derived Frequency	Virtex-5 pin#
U40	100 MHz	CLK_100MHZ	100 MHz	H17
Y1	24 MHz	USB_IFCLK	30, 48 MHz	K31
Y2	25 MHz	CLK_SYNTH0_P	25 – 700 MHz	E4
		CLK_SYNTH0_N		D4
		CLK_SYNTH0_1P		AL5
		CLK_SYNTH0_1N		AL4
Y3	25 MHz	GMII_AUX_RX_CLK	2.5, 25 MHz	AH18
		GMII_AUX_TX_CLK		AF18
		GBE_AUX_MCLK	125 MHz	AH17
Y4	25 MHz	CLK_SYNTH1_P	25 – 700 MHz	D8
		CLK_SYNTH1_N		C8
		CLK_SYNTH1_1P		AL7
		CLK_SYNTH1_1N		AM7
Y5	25 MHz	GMII_FP_RX_CLK	2.5, 25 MHz	G15
		GMII_FP_TX_CLK		K18
		GBE_FP_MCLK	125 MHz	K17

Table 17 - On-Board Clock Sources

In addition to the 100MHz oscillator, an 8-pin DIP clock socket is provided on the board so the user can supply their own oscillator of choice. The socket is a single-ended, LVTTL or LVCMOS compatible clock input to the FPGA that can be used as an alternate source for the system clock.

Signal Name	Socket pin#
Enable	1
GND	4
Output	5
VDD	8

Table 18 - Clock Socket "U23" Pin-out

There are two pairs of SMA connectors for user supplied differential clocks. The first pair is connected to the dedicated GTP clock input pins to provide a reference clock to the transceivers as shown in Figure 4 in Section 2.3. The reference designators for these connectors are “J13” and “J14”. The silk screen labels indicate the polarity of the inputs with a trailing minus sign for the N pin and a positive sign for the P pin. These differential clock inputs are AC coupled to the Virtex-5 MGTREFCLK_116 pins. The other pair of SMA connectors is connected to global clock input pins for general purpose use. The P-side connector could alternatively be used for a single-ended clock. If supplying a differential clock to the SMA connectors labeled “J11” and “J12”, make sure the jumper on “JP19" is set for 2.5V and limit the peak-to-peak voltage to 2.5V.

Net Name	Input Type	Connector.pin#	Virtex-5 pin#
CLK_SOCKET	Global clock	U23.5	J14
GREFCLK_P	Global clock	J11.1	H19
GREFCLK_N		J12.1	H20
CLK_SMA_N	GTP clock	J13.1	H3
CLK_SMA_P		J14.1	H4

Table 19 - User Clock Inputs

2.4.1 ICS8442 Programmable LVDS Clock Synthesizer

The Virtex-5 LXT/SXT PCI Express development board design uses the ICS8442 LVDS frequency synthesizer for generating various clock frequencies. A list of features included in the ICS8442 device is shown below.

- Output frequency range: 25MHz to 700MHz
- RMS period jitter: 2.7ps (typical)
- Cycle-to-cycle jitter: 27ps (typical)
- Output rise and fall time: 650ps (maximum)
- Output duty cycle: 48/52

The following figure shows a high-level block diagram of the ICS8442 programmable LVDS clock synthesizer.

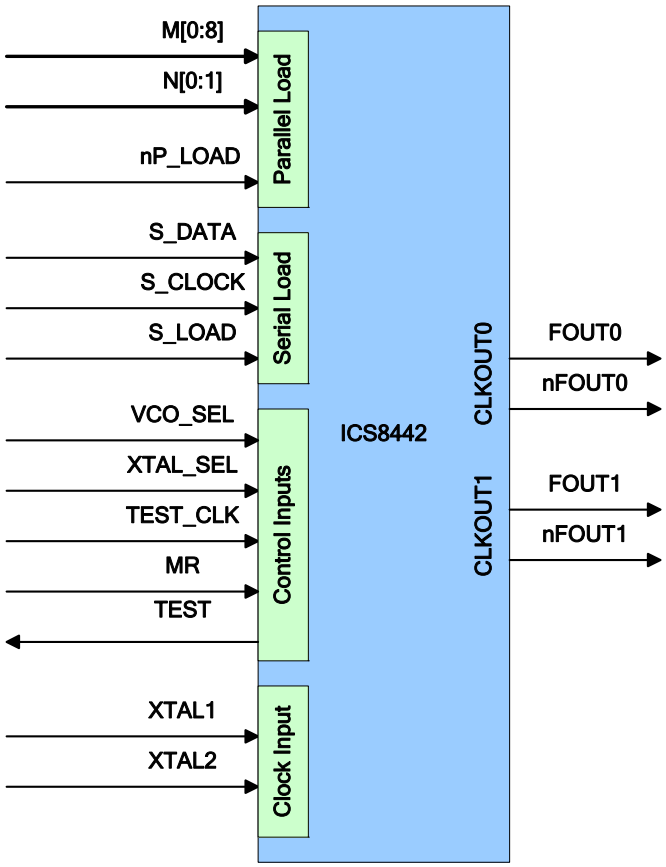


Figure 12 - ICS8442 Clock Synthesizer

Signal Name	Direction	Pull up/Pull down	Description
M[0:4], M[6:8]	Input	Pull down	The M divider inputs, latched on the rising edge of the nP_LOAD signal.
M[5]	Input	Pull up	
N[0:1]	Input	Pull down	The N divider inputs, latched on the rising edge of the nP_LOAD signal.
TEST	Output		The TEST output is active during the serial mode of operations. Please refer to the datasheet for more information.
MR	Input	Pull down	Active high reset signal.
S_CLOCK	Input	Pull down	Serial interface clock input. Data is shifted into the device on the rising edge of this clock.
S_DATA	Input	Pull down	Serial interface data input.

S_LOAD	Input	Pull down	Serial interface load signal. The contents of the serial data shift register is loaded into the internal dividers on the rising edge of this signal.
TEST_CLK	Input	Pull down	Test clock input.
nP_LOAD	Input	Pull down	The rising edge of this signal is used to load the M and N divider inputs into the device.
XTAL1, XTAL2	Input		Crystal clock input/output
XTAL_SEL	Input	Pull up	This signal is used to select between the crystal and the TEST_CLK input to the device. When this high, crystal is selected.
VCO_SEL	Input	Pull up	This signal is used to place the internal PLL in the bypass mode. When this signal is set to low, the PLL is placed in the bypass mode. For normal operations, this signal must be set to high.
FOUT0, FOUT1	Output		Positive LVDS clock outputs
nFOUT0, nFOUT1	Output		Negative LVDS clock outputs

Table 20 - ICS8442 Clock Synthesizer Pin Description

The Input Clock Select signals of the ICS8442, "VCO_SEL" and "XTAL_SEL", are not used on the Virtex-5 LXT/SXT PCI Express board. The internal pull-ups of these pins put the ICS8842 in normal operation mode where the 25MHz crystal is used as the reference clock to generate the output clocks. None of the serial input control signals are connected on the board. Programming the ICS8442 device is only possible using the M/N DIP switches on the board as indicated in the following sections.

2.4.1.1 ICS8442 Clock Generation

The ICS8442 output clocks are generated based on the following formula (assuming the crystal clock input is set to 25MHz):

FOUT[0:1] = 25 x M/N

Where 8 < M < 28 and N can take a value of 1, 2, 4, or 8. The variable M is determined by setting the binary number M[0:8] while N is set according to the following table:

N[1:0]	N	Output Clock Frequency Range (MHz)	
		Minimum	Maximum
00	1	200	700
01	2	100	350
10	4	50	175
11	8	25	87.5

Table 21 - ICS8442 N Settings

For example, to generate a 62.5MHz clock, N[1:0] will be set to "10" (it can also be set to "11" since either one will be the correct frequency range for the 62.5MHz clock) and M will be set to "000001010" (decimal 10). So, from the above formula:

FOUT[0:1] = 25 x 10/4 = 62.5Mhz

The following table shows how the M and N values can be set to generate a clock source for a few common applications. All the values for M and N are based on the 25MHz crystal clock input to the ICS8442 device. A complete list of frequencies generated by the ICS8442 (based on a 25MHz input clock) is provided in the following sections.

Interconnect Technology	FOUT0 and FOUT1 (MHz)	ICS8442 M and N Settings										
		M8	M7	M6	M5	M4	M3	M2	M1	M0	N1	N0
Gigabit Ethernet	125	0	0	0	0	0	1	0	1	0	0	1
Fiber Channel	106.25	0	0	0	0	1	0	0	0	1	1	0
	212.5	0	0	0	0	1	0	0	0	1	0	1
Infiniband	250	0	0	0	0	0	1	0	1	0	0	0
XAUI	312.5	0	0	0	0	1	1	0	0	1	0	1

Table 22 - Examples of the ICS8442 M and N Settings

2.4.1.2 ICS8442 M and N Settings

The following figure shows how the ICS8442 programmable LVDS clock synthesizer is used on the Virtex-5 LXT/SXT PCI Express board. To limit the number of required Virtex-5 I/O pins, only Parallel Mode is supported. DIP switches are provided on the board for the manual setting of the M and N values for each ICS8442.

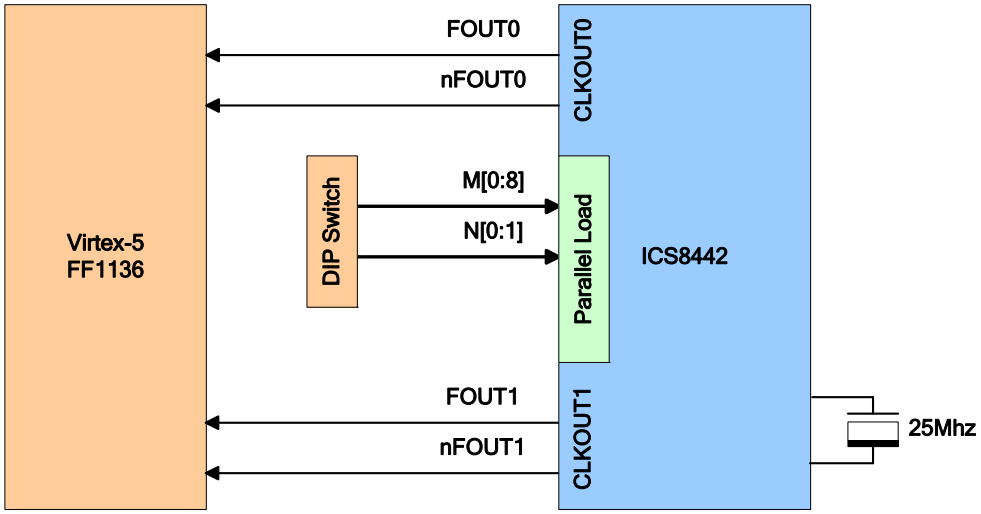


Figure 13 - ICS8442 Clock Synthesizer Interface to the FPGA

As shown in the above figure, the ICS8442 device outputs two identical LVDS clock sources. Both of these clock sources can be used to provide the reference clocks to the GTP transceivers on the Virtex-5 LXT/SXT PCI Express development board. These reference clocks could also be passed to the SMA output connectors to be used to trigger a scope during testing of the transceiver link. Likewise the SMA outputs could be used to provide an LVDS clock source to a user board.

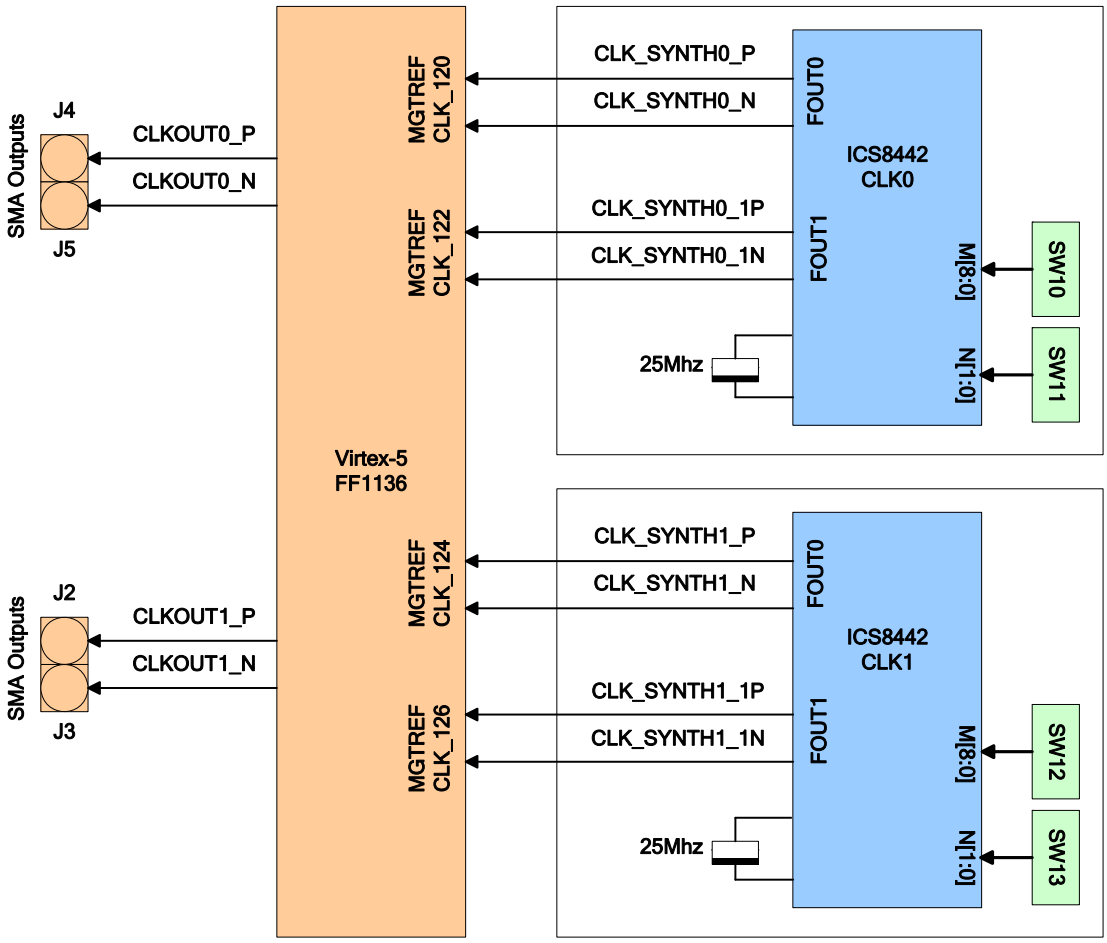


Figure 14 - ICS8442 Clock Synthesizer M and N DIP Switches

The following tables show the DIP switch settings for M and N selections. Please refer to Table 16 for the information on pull-up and pull-down resistors provided internal to the ICS8442 device for the M and N input signals.

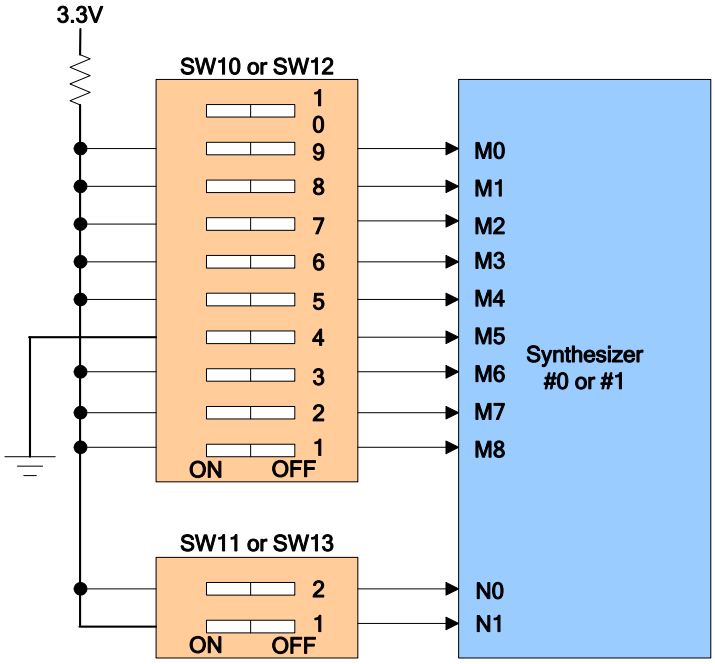


Figure 15 - M and N DIP Switches for the Synthesizers

SW10 and SW12	M[8:0]	Switch Position	
		OFF	ON
DIP1	M8	0	1
DIP2	M7	0	1
DIP3	M6	0	1
DIP4	M5	1	0 Note (1)
DIP5	M4	0	1
DIP6	M3	0	1
DIP7	M2	0	1
DIP8	M1	0	1
DIP9	M0	0	1
DIP10	Unused	NA	NA

Note(1) – The polarity of M5 (DIP4) is the opposite of all other DIP switch positions.

Table 23 - DIP Switch Setting for M[8:0]

SW11 and SW13	N[1:0]	Switch Position	
		OFF	ON
DIP1	N1	0	1
DIP2	N0	0	1

Table 24 - DIP Switch Setting for N[1:0]

The following table shows a complete list of frequencies generated by the ICS8442 device based on a 25MHz crystal reference clock input.

M[8:0]	N[1:0]	FOUT[1:0] (MHz)	M[8:0]	N[1:0]	FOUT[1:0] (MHz)
000001000	11	25 (Min)	000011000	10	150
000001001	11	28.125	000011001	10	156.25
000001010	11	31.25	000001101	01	162.5
000001011	11	34.375	000011010	10	162.5
000001100	11	37.5	000011011	10	168.75
000001101	11	40.625	000001110	01	175
000001110	11	43.75	000011100	10	175
000001111	11	46.875	000001111	01	187.5
000001000	10	50	000001000	00	200
000010000	11	50	000010000	01	200
000010001	11	53.125	000010001	01	212.5
000001001	10	56.25	000001001	00	225
000010010	11	56.25	000010010	01	225
000010011	11	59.375	000010011	01	237.5
000001010	10	62.5	000001010	00	250
000010100	11	62.5	000010100	01	250
000010101	11	65.625	000010101	01	262.5
000001011	10	68.75	000001011	00	275
000010110	11	68.75	000010110	01	275
000010111	11	71.875	000010111	01	287.5
000001100	10	75	000001100	00	300
000011000	11	75	000011000	01	300
000011001	11	78.125	000011001	01	312.5
000001101	10	81.25	000001101	00	325
000011010	11	81.25	000011010	01	325
000011011	11	84.375	000011011	01	337.5
000001110	10	87.5	000001110	00	350
000011100	11	87.5	000011100	01	350
000001111	10	93.75	000001111	00	375
000001000	01	100	000010000	00	400
000010000	10	100	000010001	00	425
000010001	10	106.25	000010010	00	450
000001001	01	112.5	000010011	00	475
000010010	10	112.5	000010100	00	500
000010011	10	118.75	000010101	00	525
000001010	01	125	000010110	00	550
000010100	10	125	000010111	00	575
000010101	10	131.25	000011000	00	600
000001011	01	137.5	000011001	00	625
000010110	10	137.5	000011010	00	650
000010111	10	143.75	000011011	00	675
000001100	01	150	000011100	00	700 (Max)

Table 25 - Synthesizer Clock Outputs for M and N Values

The following table shows the FPGA pin assignments for the primary outputs and the connectors used for the secondary outputs.

Net Name	I/O Type	Connector.pin#	Virtex-5 pin#
CLK_SYNTH0_P	FPGA input	-	E4
CLK_SYNTH0_N		-	D4
CLK_SYNTH0_1P	FPGA input	-	AL5
CLK_SYNTH0_1N		-	AL4
CLKOUT0_P	SMA output	J4.1	AK7
CLKOUT0_N		J5.1	AK6
CLK_SYNTH1_P	FPGA input	-	D8
CLK_SYNTH1_N		-	C8
CLK_SYNTH1_1P	FPGA input	-	AL7
CLK_SYNTH1_1N		-	AM7
CLKOUT1_P	SMA output	J2.1	V10
CLKOUT1_N		J3.1	V9

Table 26 - ICS8442 Pin Assignments

2.5 Communication

The Virtex-5 LXT/SXT FPGA has access to Ethernet, USB and RS232 physical layer transceivers for communication purposes. Network access is provided by two 10/100/1000 Mb/s Ethernet PHY devices, which are connected to the Virtex-5 via standard GMII interfaces. The PHY devices connect to the outside world with standard RJ45 connectors. The primary connector is located on the PCI faceplate. The auxiliary connector is only accessible if the PC cover is left open or if the board is used standalone (not plugged into a PC). General purpose I/O transfers are supported by way of the USB 2.0 port. The USB Type B peripheral connector on the faceplate facilitates communication with the board while enclosed in a PC case. Serial port communication to the embedded PowerPC processor or FPGA fabric is provided through a dual-channel RS232 transceiver.

2.5.1 10/100/1000 Ethernet PHY

The PHY devices are National DP83865DVH Gig PHYTER® V. The DP83865 is a low power version of National's Gig PHYTER V with a 1.8V core voltage and a selectable I/O voltage (2.5V or 3.3V). The PHY is connected to a Tyco RJ-45 jack with integrated magnetics (part number: 1-6605833-1). The jack also integrates two LEDs and their corresponding resistors as well as several other passive components. External logic is used to logically OR the three link indicators for 10, 100 and 1000 Mb/s to drive a Link LED on the RJ-45 jack. The external logic is for the default strap options and may not work if the strap options are changed. Four more LEDs are provided on the board for status indication. These LEDs indicate Link at 10 Mb/s, Link at 100 Mb/s, Link at 1000 Mb/s and Full Duplex operation. The PHY clock is generated from its own 25 MHz crystal. The following figure shows a high-level block diagram of the interface to the DP83865 Tri-mode Ethernet PHY.

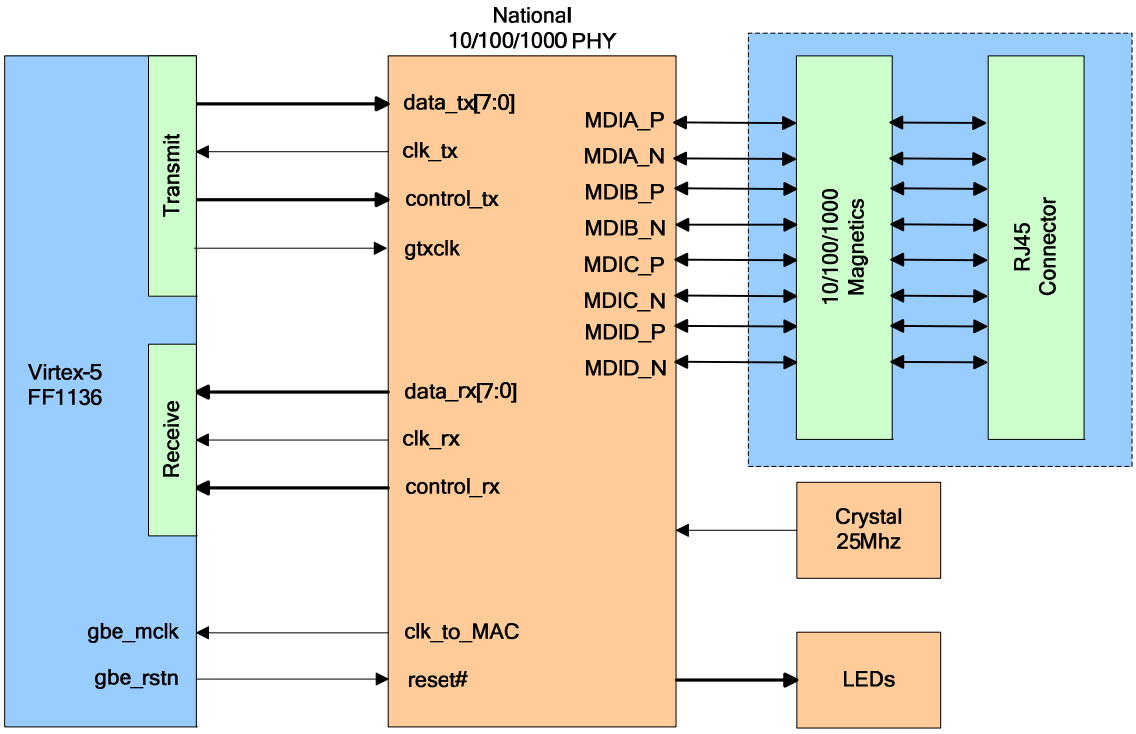


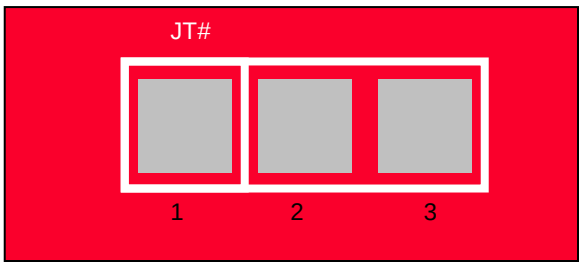
Figure 16 - 10/100/1000 Mb/s Ethernet Interface

Both PHY devices have the same address, 0b00001 by default, since they have separate, dedicated management interfaces. PHY address 0b00000 is reserved for a test mode and should not be used. Three-pad resistor jumpers are used to set the strapping options. These jumper pads provide the user with the ability to change the settings by moving the resistors. The strapping options used for both PHY devices are shown in the following table. The dual-function pins that are used for both a strapping option and to drive an LED, have a set of two jumpers per pin. The dual-function pins are indicated by an asterisk in the table.

Function	Jumper Installation		Resistor	Mode Enabled
	Faceplate (U25)	Auxiliary (U12)		
Auto-Negotiation*	JT21: pins 1-2 JT22: pins 1-2	JT3: pins 1-2 JT4: pins 1-2	0 ohm 0 ohm	Auto-negotiation enabled (default)
	JT21: pins 2-3 JT22: pins 2-3	JT3: pins 2-3 JT4: pins 2-3	0 ohm 0 ohm	Auto-negotiation disabled
Full/Half Duplex*	JT23: pins 1-2 JT24: pins 1-2	JT5: pins 1-2 JT6: pins 1-2	0 ohm 0 ohm	Full Duplex (default)
	JT23: pins 2-3 JT24: pins 2-3	JT5: pins 2-3 JT6: pins 2-3	0 ohm 0 ohm	Half Duplex
Speed 1*	JT25: pins 1-2 JT26: pins 1-2 (Speed1 – 0)	JT7: pins 1-2 JT8: pins 1-2 (Speed1 – 0)	0 ohm 0 ohm	Speed Selection: (Auto-Neg enabled) Speed1 Speed0 Speed Advertised 1 1 1000BASE-T, 10BASE-T 1 0 1000BASE-T 0 1 1000BASE-T, 100BASE-TX 0 0 1000BASE-T, 100BASE-TX, 10BASE-T Default: 1000BASE-T, 100BASE-TX, 10BASE-T
Speed 0*	JT29: pins 1-2 JT30: pins 1-2 (Speed0 – 0)	JT14: pins 1-2 JT15: pins 1-2 (Speed0 – 0)	0 ohm 0 ohm	
PHY address 0*	JT27: pins 1-2 JT28: pins 1-2	JT10: pins 1-2 JT12: pins 1-2	0 ohm 0 ohm	PHY Address 0b00001 (default)
	JT27: pins 2-3 JT28: pins 2-3	JT10: pins 2-3 JT12: pins 2-3	0 ohm 0 ohm	PHY Address 0b00000
Non-IEEE Compliant Mode	JT34: pins 1-2	JT9: pins 1-2	1 K	Compliant and Non-comp. Operation (default)
	JT34: pins 2-3	JT9: pins 2-3	1 K	Inhibits Non-compliant operation
Manual MDIX Setting	JT35: pins 1-2	JT11: pins 1-2	1 K	Straight Mode (default)
	JT35 pins 2-3	JT11 pins 2-3	1 K	Cross-over Mode
Auto MDIX Enable	JT32: pins 1-2	JT17: pins 1-2	1 K	Automatic Pair Swap – MDIX (default)
	JT32: pins 2-3	JT17: pins 2-3	1 K	Set to manual preset – Manual MDIX Setting (JT12)
Multiple Node Enable	JT31: pins 1-2	JT16: pins 1-2	1 K	Single node – NIC (default)
	JT31: pins 2-3	JT16: pins 2-3	1 K	Multiple node priority – switch/hub
Clock to MAC Enable	JT33: pins 1-2	JT18: pins 1-2	1 K	CLK_TO_MAC output enabled (default)
	JT33: pins 2-3	JT18: pins 2-3	1 K	CLK_TO_MAC output disabled

Table 27 - Ethernet PHY Hardware Strapping Options

The default options as indicated in Table 25 are Auto-Negotiation enabled, Full Duplex mode, Speed advertised as 10/100/1000 Mb/s, PHY address 0b00001, IEEE Compliant and Non-compliant support, straight cable in non-MDIX mode, auto-MDIX mode enabled, Single node (NIC) and CLK_TO_MAC enabled. The pin-out for a jumper pad is shown below.



The auto-MDIX mode provides automatic swapping of the differential pairs. This allows the PHY to work with either a straight-through cable or crossover cable. Use a CAT-5e or CAT-6 Ethernet cable when operating at 1000 Mb/s (Gigabit Ethernet). The boundary-scan Test Access Port (TAP) controller of the DP83865 must be in reset for normal operation. This active low reset pin of the TAP (TRST) is pulled low through a 1K resistor on the board.

The following tables provide the Virtex-5 pin assignments for the Ethernet PHY interfaces.

Net Name	Virtex-5 pin#		Net Name	Virtex-5 pin#
GBE_FP_MDC	H5		GBE_FP_INT#	H7
GBE_FP_MDIO	J5		GBE_FP_RST#	J7
GBE_FP_MCLK	K17		GMII_FP_CRS	T9
GMII_FP_GTC_CLK	P7		GMII_FP_COL	P10
GMII_FP_TXD0	J6		GMII_FP_RXD0	P5
GMII_FP_TXD1	K7		GMII_FP_RXD1	P6
GMII_FP_TXD2	L5		GMII_FP_RXD2	R6
GMII_FP_TXD3	K6		GMII_FP_RXD3	T6
GMII_FP_TXD4	L4		GMII_FP_RXD4	N7
GMII_FP_TXD5	L6		GMII_FP_RXD5	R7
GMII_FP_TXD6	M5		GMII_FP_RXD6	U7
GMII_FP_TXD7	M6		GMII_FP_RXD7	R8
GMII_FP_TX_EN	M7		GMII_FP_RX_DV	T8
GMII_FP_TX_ER	N5		GMII_FP_RX_ER	N8
GMII_FP_TX_CLK	K18		GMII_FP_RX_CLK	G15

Table 28 – Faceplate Ethernet PHY "U25" Pin Assignments

Net Name	Virtex-5 pin#		Net Name	Virtex-5 pin#
GBE_AX_MDC	F26		GBE_AX_INT#	F25
GBE_AX_MDIO	G27		GBE_AX_RST#	G26
GBE_AX_MCLK	AH17		GMII_AX_CRS	P24
GMII_AX_GTC_CLK	G25		GMII_AX_COL	N24
GMII_AX_TXD0	L24		GMII_AX_RXD0	K24
GMII_AX_TXD1	J24		GMII_AX_RXD1	J25
GMII_AX_TXD2	J26		GMII_AX_RXD2	J27
GMII_AX_TXD3	M28		GMII_AX_RXD3	K28
GMII_AX_TXD4	K27		GMII_AX_RXD4	L28
GMII_AX_TXD5	N28		GMII_AX_RXD5	M26
GMII_AX_TXD6	N27		GMII_AX_RXD6	L26
GMII_AX_TXD7	M27		GMII_AX_RXD7	K26
GMII_AX_TX_EN	P26		GMII_AX_RX_DV	M25
GMII_AX_TX_ER	P27		GMII_AX_RX_ER	L25
GMII_AX_TX_CLK	AF18		GMII_AX_RX_CLK	AH18

Table 29 - Auxiliary Ethernet PHY "U12" Pin Assignments

2.5.2 Universal Serial Bus (USB)

The Virtex-5 LXT/SXT PCI Express Board includes a Cypress EZ-USB FX2™ USB Microcontroller, part number CY7C68013A-100AC. The EZ-USB FX2 device is a single-chip integrated USB 2.0 transceiver, Serial Interface Engine (SIE) and 8051 microcontroller. This device supports full-speed (12 Mbps) and high-speed (480 Mbps) modes, but does not support low-speed mode (1.5 Mbps). The FX2 interface to the Virtex-5 FPGA is a programmable state machine that supports 8- or 16-bit parallel data transfers. This interface is called the General Programmable Interface (GPIF). The GPIF is controlled by Waveform Descriptors that are created with the Cypress "GPIFTool" utility and downloaded to the FX2 over the USB cable. The GPIF descriptors are stored in internal RAM and are loaded by the firmware during initialization. The GPIF interface is made up of the signals in the following table, which are connected to Virtex-5 FPGA. The USB FX2 device can also be used in a slave mode where the FPGA accesses the FX2 like a FIFO. For more information about the FX2 modes of operation, see the "EZ-USB FX2 Technical Reference Manual" and the FX2 datasheet available on Cypress Semiconductor's web site (http://www.cypress.com).

Some of the additional GPIF pins are connected to the SelectMAP configuration port on the Virtex-5 FPGA. Avnet has designed a Windows utility program that can utilize this connection to the SelectMAP port to update the FPGA configuration over the USB port. The additional pins used for the SelectMAP interface are shaded in the table. The Virtex-5 LXT/SXT PCI Express board should be used with version 3.2 or later of the "ADS USB Utility". This program can be downloaded from the

Design Resource Center (www.em.avnet.com/drc). The USB Utility only supports bit files generated with CCLK as the start-up clock.

FX2 Signal	Net Name	Virtex-5 pin#	Description
CTL[0]	USB_CTL0	N29	Control output or Slave-FIFO Flag A (Level#)
CTL[1]	USB_CTL1	N30	Control output or Slave-FIFO Flag B (Full#)
CTL[2]	USB_CTL2	P30	Control output or Slave-FIFO Flag C (Empty#)
CTL[3]	CTL3_PROG#	-	Output enable for FPGA_PROG# driver
CTL[4]	CTL4_CS#	-	SelectMAP chip select when USB_CFG_EN# low
CTL[5]	CTL5_RDWR#	-	SelectMAP write enable when USB_CFG_EN# low
RDY[0]	USB_RDY0	J30	Sample-able ready inputs
RDY[1]	USB_RDY1	J29	
RDY[2]	FPGA_BUSY	-	SelectMAP port busy indication
RDY[3]	FPGA_DONE	-	FPGA configuration DONE pin
RDY[4]	FPGA_INIT#	-	FPGA initialization pin
FD[0]	USB_FD0 (D0)	AD19	Bidirectional FIFO data bus (also SelectMAP data)
FD[1]	USB_FD1 (D1)	AE19	
FD[2]	USB_FD2 (D2)	AE17	
FD[3]	USB_FD3 (D3)	AF16	
FD[4]	USB_FD4 (D4)	AD20	
FD[5]	USB_FD5 (D5)	AE21	
FD[6]	USB_FD6 (D6)	AE16	
FD[7]	USB_FD7 (D7)	AF15	
FD[8]	USB_FD8 (D8)	AH13	Bidirectional FIFO data bus (also SelectMAP data)
FD[9]	USB_FD9 (D9)	AH14	
FD[10]	USB_FD10 (D10)	AH19	
FD[11]	USB_FD11 (D11)	AH20	
FD[12]	USB_FD12 (D12)	AG13	
FD[13]	USB_FD13 (D13)	AH12	
FD[14]	USB_FD14 (D14)	AH22	
FD[15]	USB_FD15 (D15)	AG22	
GPIFADR[0]	USB_PC0	-	Optional FPGA_CCLK out – see JT13 selection
GPIFADR[1]	FPGA_M2	-	SelectMAP port mode - M2
GPIFADR[2]	FPGA_M1	-	SelectMAP port mode - M1
GPIFADR[3]	FPGA_M0	-	SelectMAP port mode - M0
GPIFADR[4]	JTAG_TDI	-	Optional JTAG interface – TDI (install RP3)
GPIFADR[5]	JTAG_TDO	-	Optional JTAG interface – TDO (install RP3)
GPIFADR[6]	JTAG_TMS	-	Optional JTAG interface – TMS (install RP3)
GPIFADR[7]	JTAG_TCK	-	Optional JTAG interface – TCK (install RP3)
IFCLK	USB_IFCLK	K31	Interface clock, optional FPGA_CCLK (JT13)
PA0/INT0#	USB_INT0#	M30	Port A I/O or active-low interrupt 0
PA1/INT1#	USB_INT1#	M31	Port A I/O or active-low interrupt 1
PA2/SLOE	USB_SLOE	L30	Port A I/O or slave-FIFO output enable
PA3/WU2	USB_WU2	L31	Port A I/O or alternate wake-up pin
PA4/FIFOADR0	USB_FA0	K29	Port A I/O or slave-FIFO address select 0
PA5/FIFOADR1	USB_FA1	L29	Port A I/O or slave-FIFO address select 1
PA6/PKTEND	USB_PEND	J31	Port A I/O or slave-FIFO packet end
PA7/SLCS#	USB_SLCS#	P29	Port A I/O or slave-FIFO enable
RESET#	USB_RST#	P31	USB device active-low reset

Table 30 - USB Interface FPGA Pin-out

2.5.3 RS232

The RS232 transceiver is a 3222 available from Harris/Intersil (ICL3222CA) and Analog Devices (ADM3222). This transceiver operates at 3.3V with an internal charge pump to create the RS232 compatible output levels. This level converter supports two channels. The primary channel is used for transmit and receive data (TXD and RXD). The secondary channel may be connected to the FPGA by installing jumpers on “JP4” and “JP7” for use as CTS and RTS signals. The RS232 console interface is brought out on the DB9 connector labeled “J8”. The Virtex-5 LXT/SXT PCI Express board supports both straight-through and null-modem serial cables by selecting the DB9 pin-out with the 3-pin jumper headers labeled “JP3” and “JP6” as shown in the following figure.

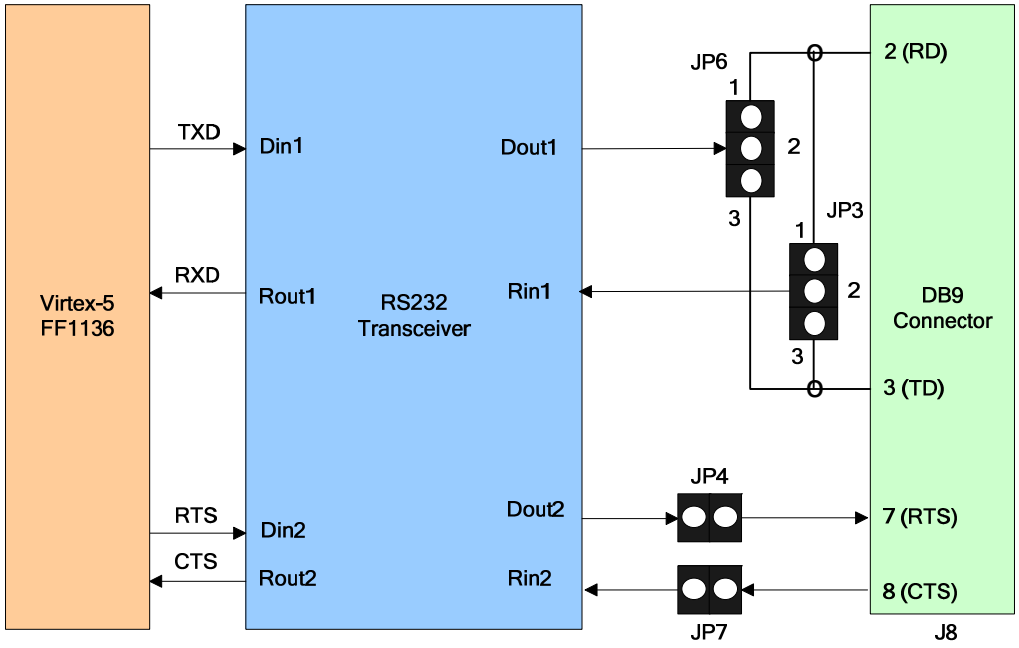


Figure 17 - RS232 Interface

A male-to-female serial cable should be used to plug "J8" into a standard PC serial port (male DB9). The following tables show the FPGA pin-out and jumper settings for the RS232 interface.

Net Name	Description	Virtex-5 Pin #
RS232_RXD	Received Data, RD	R31
RS232_TXD	Transmit Data, TD	U30
RS232_RTS	Request To Send, RTS	T31
RS232_CTS	Clear To Send, CTS	R29

Table 31 - RS232 Signals

Mode of Operation	JP3	JP6	Cable
DCE (default)	Install a jumper on pins 2-3	Install a jumper on pins 1-2	Straight-thru
DTE	Install a jumper on pins 1-2	Install a jumper on pins 2-3	Null-modem

Table 32 - RS232 Port Jumper Settings

2.6 User Switches

Four momentary closure push buttons have been installed on the board and attached to the FPGA. These buttons can be programmed by the user and are ideal for logic reset and similar functions. Pull down resistors hold the signals low until the switch closure pulls them high (active high signals).

Net Name	Reference	Virtex-5 Pin #
SWITCH_PB1	SW2	AM32
SWITCH_PB2	SW3	AN34
SWITCH_PB3	SW4	AN33
SWITCH_PB4	SW5	AN32

Table 33 - Push Button Pin Assignments

An eight-position dipswitch (SPST) has been installed on the board and attached to the FPGA. These switches provide digital inputs to user logic as needed. The signals are pulled low by 1K ohm resistors when the switch is open and tied high to 3.3V when closed as shown in the following table.

Net Name	Reference	Voltage when closed	Virtex-5 Pin#
SWITCH0	SW7 – 1	3.3V	U26
SWITCH1	SW7 – 2		U27
SWITCH2	SW7 – 3		U28
SWITCH3	SW7 – 4		T28
SWITCH4	SW7 – 5		T30
SWITCH5	SW7 – 6		T29
SWITCH6	SW7 – 7		R27
SWITCH7	SW7 – 8		R26

Table 34 - DIP Switch Pin Assignments

2.7 User LEDs

Eight discrete LEDs are installed on the board and can be used to display the status of the internal logic. These LEDs are attached as shown below and are lit by forcing the associated FPGA I/O pin to a logic '1' and are off when the pin is either low (0) or not driven.

Net Name	Reference	Virtex-5 Pin#
LED0	D1	H13
LED1	D2	J17
LED2	D3	H15
LED3	D4	G16
LED4	D5	L18
LED5	D6	H18
LED6	D7	J19
LED7	D8	J21

Table 35 - LED Pin Assignments

2.8 Configuration

The Virtex-5 LXT/SXT PCI Express Board supports several methods of configuring the FPGA. The possible configuration sources include Boundary-scan (JTAG cable), Byte Peripheral Interface (parallel Flash), the Cypress USB device or the System ACE Module (SAM) header. The blue LED labeled "DONE" on the board illuminates to indicate when the FPGA has been successfully configured.

2.8.1 Configuration Modes

Upon power-up the FPGA will be enabled in a configuration mode defined by the jumper on "JP1". The default configuration mode is "Master BPI-Up" mode, which will allow the FPGA to be configured from the parallel Flash device. The Flash has been programmed with basic test application code to test the on-board peripherals. Section 3.0 describes the various tests included in the Flash. The configuration mode is selected by installing a jumper either across pins 1 and 2 or across pins 2 and 3 as shown in the following table.

Configuration Mode	JP1
Master BPI-Up	1-2
Boundary-scan	2-3

Table 36 – Setting the Configuration Mode "JP1"

Set the jumper for Boundary-scan mode to disable the FPGA from booting from the Flash device. The jumper must be set for Boundary-scan when using a System ACE Module to configure the FPGA. The mode pins are pulled up or down by weak resistors so that the Cypress USB device can override the mode selection to configure the FPGA in Slave SelectMAP mode. See Section 2.5.2 for more information on using the Cypress device to configure the FPGA.

2.8.2 JTAG Chain

The Virtex-5 LXT/SXT PCI Express Board has one device in the JTAG chain, the Virtex-5 LXT/SXT FPGA. The following figure shows a high-level block diagram of the JTAG Chain on the development board.

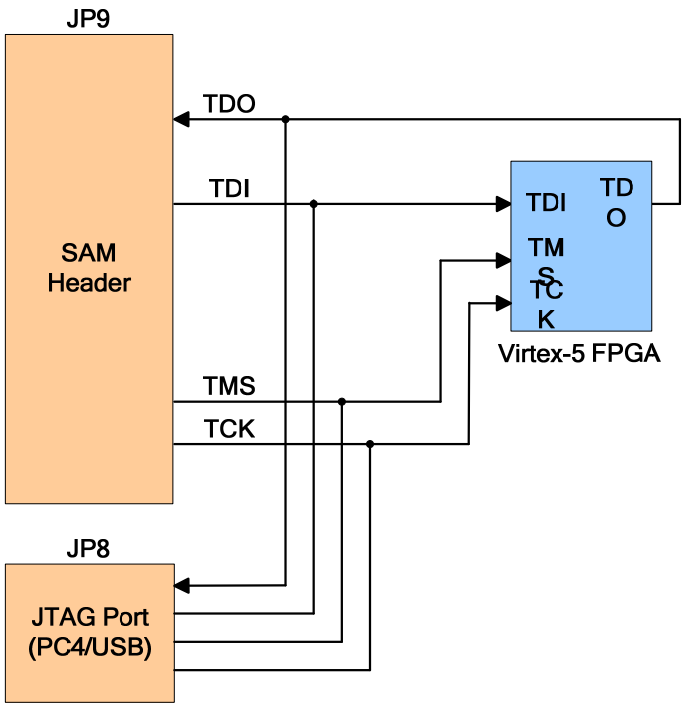


Figure 18 - JTAG Chain on the Virtex-5 PCI Express Board

Programming the Virtex-5 FPGA via Boundary-scan mode requires a JTAG download cable (not included in the kit). The Virtex-5 LXT/SXT PCI Express Board has connectors to support both the flying leads connection of the Parallel Cable III and the ribbon cable connection of the Parallel Cable IV and Platform Cable USB. These connectors are labeled "JP9" and "JP8" respectively. For more information about JTAG download cables, perform a search on the Xilinx web page http://www.xilinx.com using the key words "Programming Cables". When using the flying leads connection of the Parallel Cable III, connect the leads to SAM header as indicated in the following table.

Signal Name	JP9 pin
TDO	3
TMS	5
TDI	7
VCC	2
GND	4
TCK	10

Table 37 - Flying Lead JTAG Header

If the Parallel Cable IV or Platform Cable USB is used, the ribbon cable connector mates with keyed connector "JP8".

2.8.3 Byte Peripheral Interface (BPI)

The Flash can be re-programmed with new configuration data using a JTAG download cable and the iMPACT software that comes with the Xilinx ISE tools. The iMPACT software indirectly programs the Flash by downloading a bitstream to the FPGA that facilitates communication with the Flash device when a program operation is selected. The Flash must be erased before programming a new configuration file into the device. The PROM File Formatter in iMPACT must be used to convert the user bitstream(s) into a file format supported by the BPI Flash programmer (ex. MCS file). After the Flash has been re-programmed, pressing the pushbutton labeled "SW9" will reconfigure the FPGA with the new configuration data stored in the Flash device (assuming JP1 is set for BPI mode).

The Virtex-5 LXT/SXT PCI Express board is designed to support both MultiBoot and Fallback applications. Flash address pins A23 and A22 are connected to the Revision Select (RS[1:0]) pins, dividing the first 16MB of Flash memory into four 4MB regions for bitstream storage. The default configuration address is set by pull-up and pull-down resistors on the RS[1:0] pins. The RS[1:0] pins are set to "01" on the board, yielding a default start address of 0x400000 (the second 4MB region). The user

must use this address for the default bitstream when using the PROM File Formatter in iMPACT to generate a PROM file for use with the BPI Flash programmer.

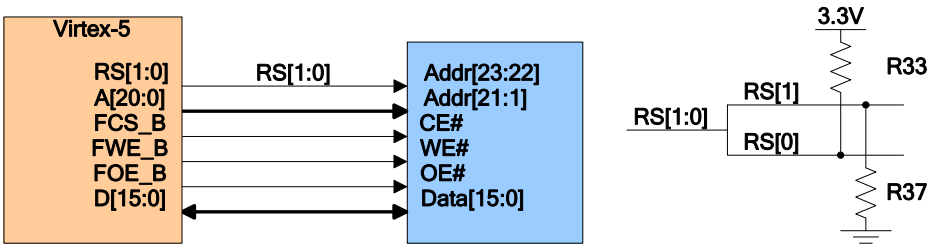


Figure 19 - Flash Connections for Fallback Reconfiguration

The least significant address pin on the Virtex-5 connects to Flash address pin A1 to support 16-bit wide configuration data. The Flash A0 pin is connected to a regular I/O pin on the FPGA but it is not used by the P30 Flash device nor required for 16-bit BPI mode.

2.8.4 System ACE Module Connector

The Virtex-5 LXT/SXT PCI Express development board provides support for the Avnet/Memec System ACE Module (SAM) via the 50-pin connector labeled "JP9" on the board. The SAM can be used to configure the FPGA or to provide bulk Flash to the logic design. The Avnet/Memec System ACE module (DS-KIT-SYSTEMACE) is sold separately. The figure below shows the System ACE Module connected to the header on the Virtex-5 LXT/SXT PCI Express board.

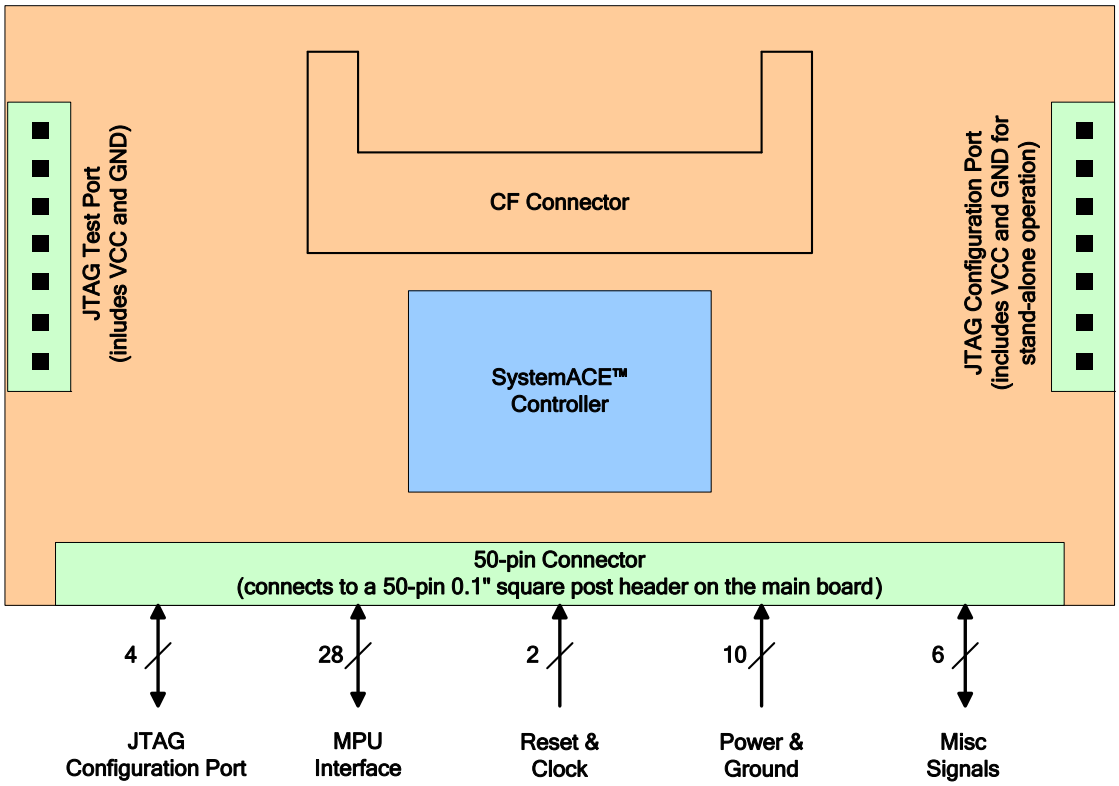


Figure 20 - SAM Interface (50-pin header)

The following table shows the System ACE ports that are accessible over the SAM header. The majority of the pins on this header may be used as general purpose I/O when not using a System ACE Module. The Virtex-5 pin numbers are provided for these general purpose pins.

Virtex-5 Pin#	System ACE Signal Name	SAM Connector Pin # (JP9)	System ACE Signal Name	Virtex-5 Pin#

-	**3.3V**	1	2	**3.3V**	**-**
-	TDO	3	4	**GND**	**-**
-	TMS	5	6	CLOCK	J20
-	TDI	7	8	**GND**	**-**
-	PROGRAMn	9	10	TCK	-
-	**GND**	11	12	**GND**	**-**
AH7	OEn	13	14	INITn	-
AH5	MPA0	15	16	WEn	AD6
AG7	MPA2	17	18	MPA1	Y9
-	**2.5V**	19	20	MPA3	Y8
AG6	MPD00	21	22	**2.5V**	**-**
AG5	MPD02	23	24	MPD01	AA6
AF6	MPD04	25	26	MPD03	Y7
AF5	MPD06	27	28	MPD05	Y6
AE7	MPD08	29	30	MPD07	W9
AE6	MPD10	31	32	MPD09	W6
AD7	MPD12	33	34	MPD11	W7
AD4	MPD14	35	36	MPD13	W10
AD5	MPA4	37	38	MPD15	V7
AC4	MPA6	39	40	MPA5	V8
AC5	IRQ	41	42	**GND**	**-**
AC7	RESETn	43	44	CEn	Y11
-	DONE	45	46	BRDY	W11
-	CCLK	47	48	BITSTREAM	-
-	**GND**	49	50	**NC**	**-**

Table 38 - SAM Interface Signals

2.9 Power

The Virtex-5 LXT/SXT PCI Express Board power is developed from a +5V input provided by the furnished power supply or derived from the +12V rail of a PCI Express bus via a Texas Instruments (TI) PTH12050W power module. The +2.5V and +3.3V power rails and +1.0V FPGA core power are developed by TI PTH5050W power modules; these modules are capable of furnishing up to 6A each. +1.8V power is developed from the +5V rail by a TI PTH5010W power module capable of furnishing up to 15A; +0.9V DDR2 reference/termination voltage is by a linear regulator from the +1.8V rail. In stand-alone mode the board is connected to the external power supply via the "J10" barrel socket connector (included 6.5A power supply), or the PC hard-drive power connector "J7" (optional power connection). The current requirements for the board are application specific. It should be noted that, per the PCI Express specification, maximum power available to a single x8 PCI Express add-in card is 25 watts (5A @+5V). For stand-alone applications, the fuse may be removed from the fuse holder "F1"; for PCI applications the fuse must be installed in the fuse holder. The figure on the following page shows a high-level block diagram of the main power supply on the development board.

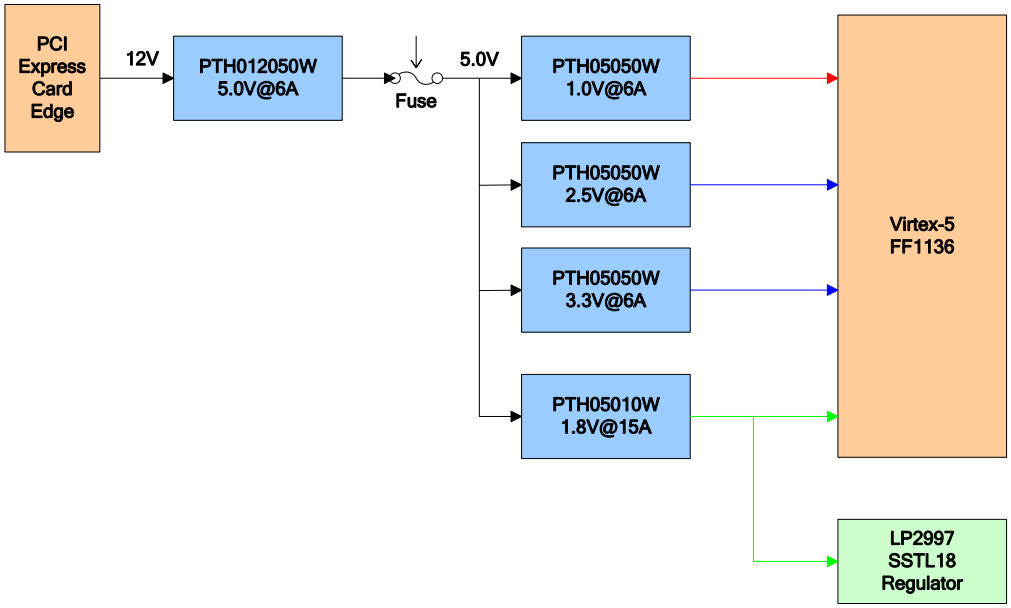


Figure 21 - Main Power Supply

2.9.1 FPGA I/O Voltage (Vcco)

FPGA banks 0 - 2, 15 and 19 are powered at VCCO = +3.3V and banks 5, 6, 17, 21, 23 and 25 are powered at VCCO = +1.8V. There are four selectable voltage rails, two for each of the two EXP connectors. The single-ended I/O for each EXP connector have an independent voltage select from the differential I/O on the connector. These selectable voltage rails may be powered at +2.5V or +3.3V using the jumpers labeled “JP16”, “JP18”, “JP19” and “JP20”.

Bank #	1.8V	3.3V	2.5V/3.3V	Selectable Rail
0		X		-
1		X		-
2		X		-
3			X	VIO_EXP1_DP
4			X	VIO_EXP2_DP
5	X			-
6	X			-
11			X	VIO_EXP1_SE
12			X	VIO_EXP1_DP
13			X	VIO_EXP2_SE
15		X		-
17	X			-
18			X	VIO_EXP2_DP
19		X		-
20			X	VIO_EXP2_DP
21	X			-
22			X	VIO_EXP2_DP
23	X			-
25	X			-

Table 39 – I/O Bank Voltages

2.9.2 FPGA Reference Voltage (Vref)

The Virtex-5 LXT/SXT PCI Express Board provides the reference voltage of +0.9V to the FPGA banks connected to the DDR2 memory interfaces.

2.9.3 GTP Voltage Regulators (AVCC, AVCCPLL, VTTRX, VTTTX, VTTRXC)

The Virtex-5 LXT/SXT PCI Express Board provides point-of-load regulation for the GTP supplies with high-precision, low drop-out linear regulators from Texas Instruments. The TPS743xx family of LDO regulators provide up to 1.5 amps of current with less than 30uVrms of output noise. The ultra-low input voltage requirement minimizes the voltage drop across the regulator saving the added cost of thermal solutions in most applications. The adjustable output range, down to 0.9V, makes the TPS74301 a good fit for the low voltage GTP supplies. The small 5mm x 5mm QFN packages are ideal for space limited applications like PCI form-factor add-in cards. The following figure shows a high-level block diagram of the GTP power supplies.

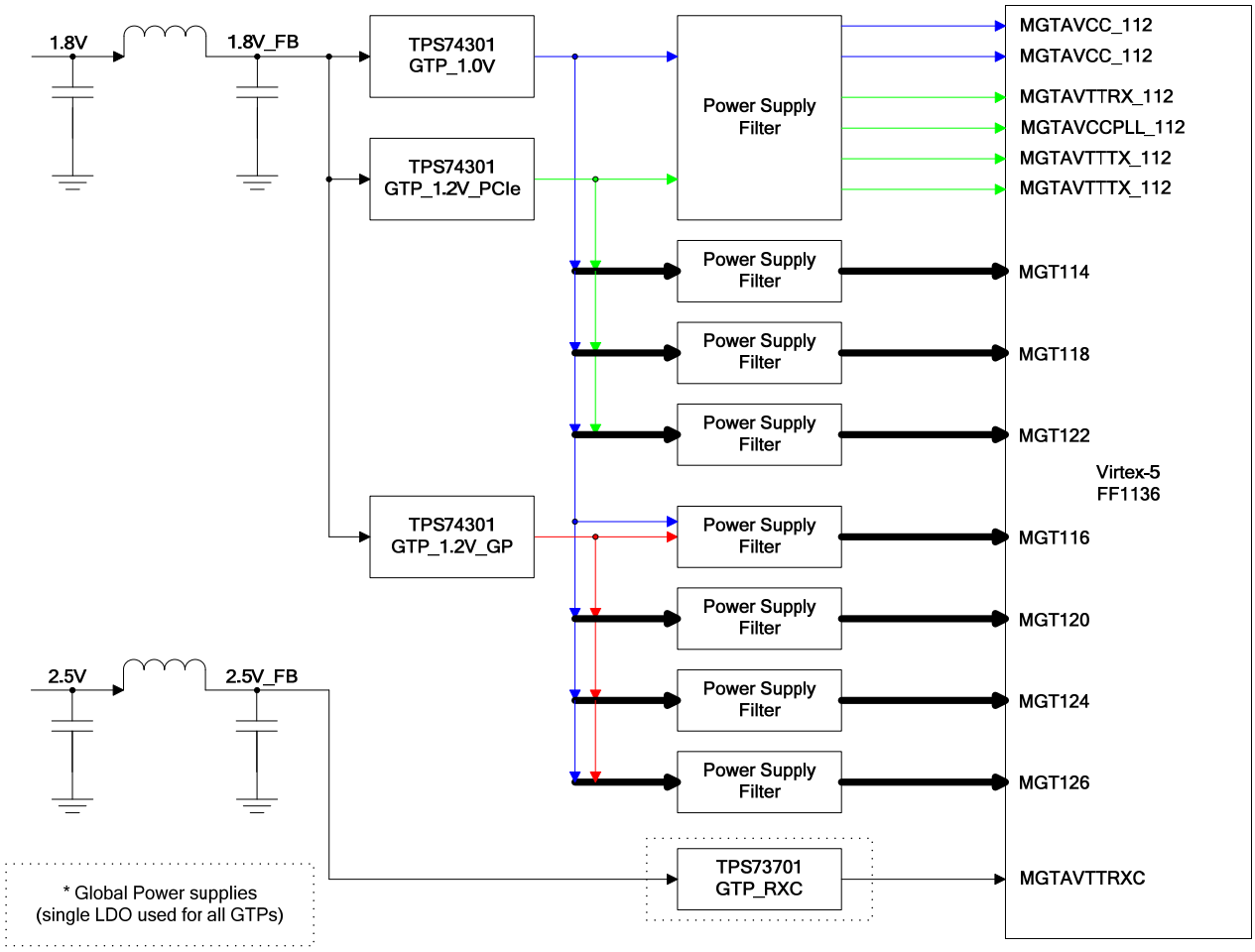


Figure 22 - GTP Voltage Regulators

The circuits for the TPS74301 regulators on the Virtex-5 LXT/SXT PCI Express board also support the footprint compatible TPS74201 and TPS74401 devices. The TPS74201 regulator has the same current capability as the TPS74301 but provides a Soft-Start function where the ramp time is set with an external capacitor instead of tracking the input rail. The TPS74401 regulator can provide double the current capability (up to 3 Amps) making the power supply scalable if more current is needed. If replacing any of the TPS74301 regulators on the board with either the TPS74201 or TPS74401, remove the 0 ohm resistor connecting the track pin to the 5V rail (R178, R182 or R186).

The GTP supply pins require 1.0 Volt or 1.2 Volts depending on the pin type. The adjustable TPS74301 regulators use an external voltage divider to set the output voltage. A single TPS74301 regulator supplies the MGTAVCC pins of every GTP_Dual tile. The remaining supply pins are separated into two power rails based on application. The "GTP_1.2V_PCIe" rail supplies the MGTAVCCPLL, MGTVTTTX and MGTVTTRX pins for the four GTP_Dual tiles used for the PCI Express interface. Likewise the "GTP_1.2V_GP" rail supplies the same type of pins for the four remaining tiles consisting of the SFP, SATA, EXP and 10 Gb/s Media interfaces. A single, adjustable TPS73701 LDO is used to supply the MGTAVTTRXC pin. The following table contains estimated current utilization for the GTP rails based on the Virtex-5 datasheet.

Net Name	MGT Rails	Current Consumption per tile		
		Min	Typical	Max
GTP_1.2V_xxx	MGTAVCCPLL	-	108 mA	151 mA
	MGTVTTTX			
	MGTVTTRX			
GTP_1.0V	MGTAVCC	-	56 mA	110 mA
GTP_RXC	MGTAVTTRXC	-	0.1 mA	0.5 mA

Table 40 - Typical Current Measurements per MGT Tile

2.10 Thermal Management

The Virtex-5 LXT/SXT FPGA on the development board requires a heat sink to keep the junction temperate within the operating limits of the device. The amount of power that needs to be dissipated is design dependent. The main contributors to the overall power are utilization, frequency and the number of active RocketIO transceivers. The board includes a passive heat sink that is adequate for moderate logic utilization and moderate frequency designs in ambient air flow. Forced air flow may be required to support designs containing more than eight active RocketIO transceivers. Even with forced air flow the passive heat sink may not be capable of dissipating the power in all applications. For designs with higher utilization, high-frequency blocks and/or more than eight active transceivers, an active heat sink may be required. The Virtex-5 LXT/SXT PCI Express provides power connectors for both 5 Volt and 12 Volt fans. The following sections provide details on the passive heat sink included with the kit and the active heat sinks supported by the board (purchased separately).

2.10.1 Passive Heat Sink

The Virtex-5 LXT/SXT PCI Express Board includes a 6 mm passive heat sink with push-pin attachment to the Virtex-5 FPGA. This heat sink is part of the Aavid Thermalloy product offering for Ball Grid Arrays (BGA). More information is available on Aavid's web site: http://www.aavidthermalloy.com/products/bga/index.shtml. A 37.4 mm x 37.4 mm heat sink is used to fit the 35 mm FF1136 package. The push-pin mounting holes in the board support the industry standard hole pattern shown below.

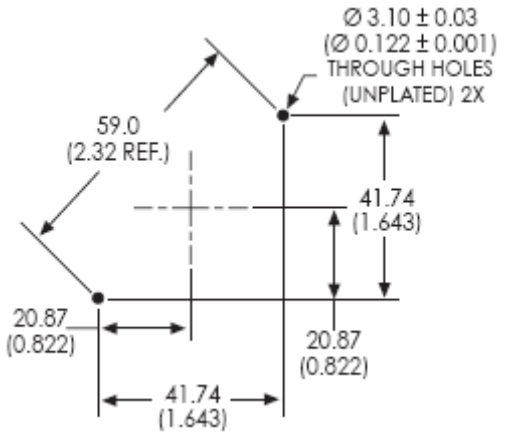


Figure 23 - Heat Sink Mounting-Hole Pattern

The part number for the Aavid Thermalloy heat sink is 372924M02000G. The 6 mm height provides enough vertical clearance to install an EXP daughter module in the board-to-board connectors straddling the Virtex-5 FPGA. The forced air flow should be directed across the length of the board if used on a bench top. Standard PC cases usually pull air across the PCI cards in this direction.

2.10.2 Active Heat Sink Support

The Virtex-5 LXT/SXT PCI Express Board supports active heat sinks with both 5V and 12V power connectors and the industry standard push-pin hole pattern. The Virtex-5 LXT/SXT PCI Express board supports up to a 40 mm x 40 mm heat sink and/or heat sink fan. The 3-pin power connector labeled "JP22" is used for 5V fans with Molex mating series 2695 and 40 mm of lead length. The 2-pin power connector labeled "JP23" is used for 12V fans with Molex mating series. The following table provides Aavid Thermalloy part numbers for recommended active heat sinks (purchased separately).

Part Number	Fan Voltage	Height	Lead Length	Thermal Resistance		Board Connector
11-5602-45	5V	15.0 mm	127 mm	3.40 C/W		JP22
11-5602-51	12V	11.5 mm	40 mm	3.70 C/W		JP23

Table 41 - Recommended Active Heat Sinks

2.11 Expansion Connectors

The Virtex-5 LXT/SXT PCI Express board provides expansion capabilities for customized user application daughter cards and interfaces over two EXP expansion connectors. The EXP expansion connectors on the board can support two half-card EXP modules, or a single dual slot EXP module. Both off-the-shelf EXP modules and user-developed modules can easily be plugged onto the Virtex-5 LXT/SXT PCI Express board to add features and functions to the backend application of the main board. For more information, view the EXP specification at www.em.avnet.com/exp.

2.11.1 EXP Interface

The EXP specification defines a 132-pin connector, with 24 power, 24 grounds, and 84 user I/Os. The standard EXP configuration implemented on the Virtex-5 LXT/SXT PCI Express board uses two connectors (Samtec part number QTE-060-09-F-D-A) in a dual slot EXP configuration, with a total of 164* user I/Os. Using a jumper, you can set the voltage levels for the EXP user I/O to either 2.5V or 3.3V. As shown in the following figure, "JP16" and "JP19" set the I/O voltage for the EXP connector labeled "JX1" while "JP18" and "JP20" set the I/O voltage for the EXP connector labeled "JX2", by setting the VCCO voltage for the banks of the FPGA that connect to the EXP I/O.

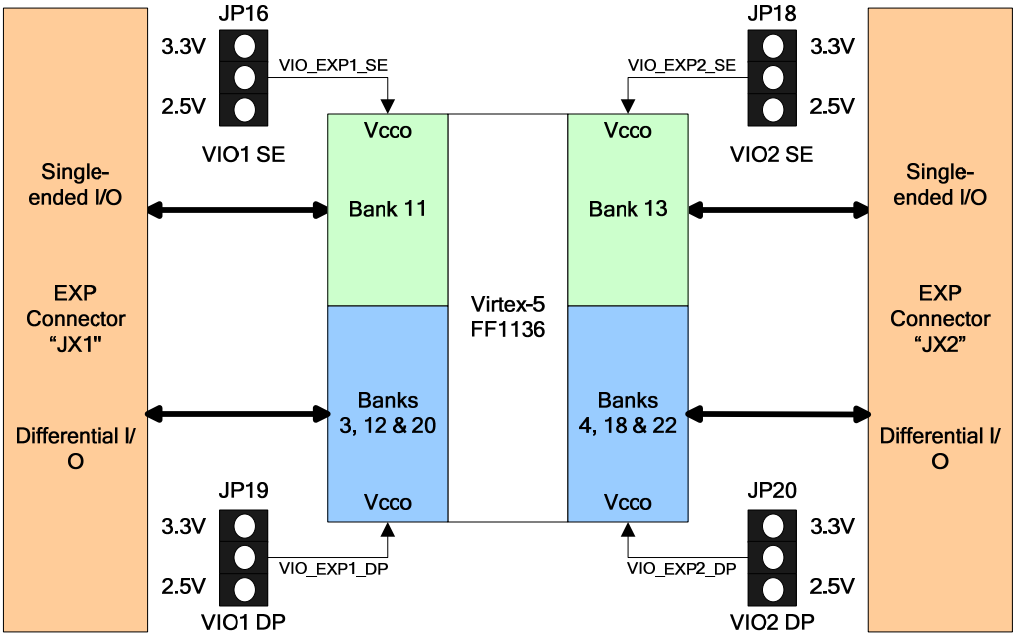


Figure 24 - EXP I/O Voltage Settings

The EXP specification defines four user signal types: Single Ended I/O, Differential I/O, Differential and Single Ended Clock Inputs, and Differential and Single Ended Clock Outputs. Because the FPGA I/Os can be configured for either single-ended or differential use, the differential I/Os defined in the EXP specification can serve a dual role. All the differential I/O signals can be configured as either differential pairs or single-ended signals, as required by the end application. In providing differential signaling, higher performance LVDS interfaces can be implemented between the baseboard and EXP module. Connection to

high speed A/Ds, D/As, and flat panel displays are possible with this signaling configuration. Applications that require single-ended signals only can use each differential pair as two single-ended signals.

Net Names	Signal Description	JX1	JX2	Total
EXPx_SE_IO	Single-ended I/O	34	34	68
EXPx_SE_CLK_IN	Single-ended clock input	1	1	2
EXPx_SE_CLK_OUT	Single-ended clock output	1	1	2
EXPx_DIFF_p/n	Differential I/O pairs	20	22	42
EXPx_DIFF_CLK_IN_p/n	Differential clock input pair, global	1	1	2
EXPx_DIFF_CLK_OUT_p/n	Differential clock output pair	1	1	2
Total		**80**	**84**	**164**

Table 42 - EXP Connector Signals

Since the Virtex-5 LXT/SXT FPGA supports regional clocking and GTP transceivers, the optional RCLK pair and MGT pairs defined in version 1.3 of the EXP specification are utilized. The "EXPx_RCLK_DIFF_p/n10" differential pairs on both "JX1" and "JX2" are connected to clock-capable pins to support regional clocking applications. Since these regional clock pairs can also be used as general purpose differential I/O pairs, they are counted as "Differential I/O pairs" in the previous table.

The alternate function of differential pairs 20 and 21 is used to connect one of the GTP transceivers to EXP connector "JX1". The "EXP1_MGT_RX_DIFF_p/n20" pair and "EXP1_MGT_TX_DIFF_p/n21" pair are connected to MGT116 transceiver #1 to support high-speed, serial communication to the daughter card. These MGT pairs are connected to "JX1" pins "54 & 56" and "53 & 55" respectively. These pins can only be used by daughter cards supporting the RocketIO transceiver link. This reduces the number of differential I/O pairs from 22 down to 20 for the EXP connector labeled "JX1". The alternate function nets defined in the EXP v1.3 specification that are supported by the Virtex-5 LXT/SXT PCI Express board are shown in the following table.

Alternate Function Nets	Signal Description	Supported?	
		JX1	JX2
EXPx_RCLK_DIFF_p/n10	Differential clock input pair, regional	Yes	Yes
EXPx_MGT_RX_DIFF_p/n20	GTP transceiver, receive pair	Yes	No
EXPx_MGT_TX_DIFF_p/n21	GTP transceiver, transmit pair	Yes	No

Table 43 - EXP v1.3 Alternate Function Pins

The Virtex-5 FPGA user I/O pins that connect to the two EXP connectors are shown in the following table. The Samtec QTE connector plugs on the Virtex-5 LXT/SXT PCI Express board (part number: QTE-060-09-F-D-A) mate with the Samtec QSE high-performance receptacles (part number: QSE-060-01-F-D-A), located on the daughter card. Samtec also provides several high-performance ribbon cables that will mate to the "JX1" and "JX2" connectors.

Virtex-5 Pin#	Net Name	EXP Connector Pin # (JX1)		Net Name	Virtex-5 Pin#
H32	EXP1_SE_IO_0	2	1	EXP1_SE_IO_1	R34
G33	EXP1_SE_IO_2	4	3	EXP1_SE_IO_3	P32
-	**2.5V**	6	5	**2.5V**	-
G32	EXP1_SE_IO_4	8	7	EXP1_SE_IO_5	N33
F34	EXP1_SE_IO_6	10	9	EXP1_SE_IO_7	N34
-	**2.5V**	12	11	**2.5V**	-
F33	EXP1_SE_IO_8	14	13	EXP1_SE_IO_9	N32
E34	EXP1_SE_IO_10	16	15	EXP1_SE_IO_11	M33
-	**2.5V**	18	17	**2.5V**	-
E33	EXP1_SE_IO_12	20	19	EXP1_SE_IO_13	M32
E32	EXP1_SE_IO_14	22	21	EXP1_SE_IO_15	L33
-	**2.5V**	24	23	**2.5V**	-
D34	EXP1_SE_IO_16	26	25	EXP1_SE_IO_17	L34
D32	EXP1_SE_IO_18	28	27	EXP1_SE_IO_19	K33
-	**2.5V**	30	29	**2.5V**	-
C34	EXP1_SE_IO_20	32	31	EXP1_SE_IO_21	K34
C33	EXP1_SE_IO_22	34	33	EXP1_SE_IO_23	K32
-	**2.5V**	36	35	**2.5V**	-
C32	EXP1_SE_IO_24	38	37	EXP1_SE_IO_25	J34
B33	EXP1_SE_IO_26	40	39	EXP1_SE_IO_27	J32
L19	EXP1_DIFF_CLK_IN_p	42	41	EXP1_SE_IO_28	H34
K19	EXP1_DIFF_CLK_IN_n	44	43	EXP1_SE_CLK_IN	H14
-	**GND**	46	45	**GND**	-
A33	EXP1_SE_IO_30	48	47	EXP1_SE_IO_29	H33
B32	EXP1_SE_IO_31	50	49	EXP1_SE_CLK_OUT	R33
-	**GND**	52	51	**GND**	**-**
K1	EXP1_MGT_RX_DIFF_p20	54	53	EXP1_MGT_TX_DIFF_p21	L2
J1	EXP1_MGT_RX_DIFF_n20	56	55	EXP1_MGT_TX_DIFF_n21	K2
-	**GND**	58	57	**GND**	**-**
G11	EXP1_DIFF_p18	60	59	EXP1_SE_IO_32	P34
G12	EXP1_DIFF_n18	62	61	EXP1_SE_IO_33	T33
-	**GND**	64	63	**GND**	**-**
E12	EXP1_DIFF_p16	66	65	EXP1_DIFF_p19	L10
E13	EXP1_DIFF_n16	68	67	EXP1_DIFF_n19	L11
-	**GND**	70	69	**GND**	**-**
T10	EXP1_DIFF_CLK_OUT_p	72	71	EXP1_DIFF_p17	F13
T11	EXP1_DIFF_CLK_OUT_n	74	73	EXP1_DIFF_n17	G13
-	**GND**	76	75	**GND**	**-**
D12	EXP1_DIFF_p14	78	77	EXP1_DIFF_p15	K11
C12	EXP1_DIFF_n14	80	79	EXP1_DIFF_n15	J11
A13	EXP1_DIFF_p12	82	81	EXP1_DIFF_p13	D11
B12	EXP1_DIFF_n12	84	83	EXP1_DIFF_n13	D10
-	**3.3V**	86	85	**3.3V**	**-**
K8	EXP1_RCLK_DIFF_p10	88	87	EXP1_DIFF_p11	F10
K9	EXP1_RCLK_DIFF_n10	90	89	EXP1_DIFF_n11	G10
-	**3.3V**	92	91	**3.3V**	**-**
B13	EXP1_DIFF_p8	94	93	EXP1_DIFF_p9	H10
C13	EXP1_DIFF_n8	96	95	EXP1_DIFF_n9	H9
-	**3.3V**	98	97	**3.3V**	**-**
F11	EXP1_DIFF_p6	100	99	EXP1_DIFF_p7	J10
E11	EXP1_DIFF_n6	102	101	EXP1_DIFF_n7	J9
-	**3.3V**	104	103	**3.3V**	**-**
E9	EXP1_DIFF_p4	106	105	EXP1_DIFF_p5	M10
E8	EXP1_DIFF_n4	108	107	EXP1_DIFF_n5	L9
-	**3.3V**	110	109	**3.3V**	**-**
F9	EXP1_DIFF_p2	112	111	EXP1_DIFF_p3	M8
F8	EXP1_DIFF_n2	114	113	EXP1_DIFF_n3	L8
-	**3.3V**	116	115	**3.3V**	**-**
G8	EXP1_DIFF_p0	118	117	EXP1_DIFF_p1	N10
H8	EXP1_DIFF_n0	120	119	EXP1_DIFF_n1	N9
-	**GND**	122	121	**GND**	**-**
-	**GND**	124	123	**GND**	**-**
-	**GND**	126	125	**GND**	**-**
-	**GND**	128	127	**GND**	**-**
-	**GND**	130	129	**GND**	**-**
-	**GND**	132	131	**GND**	**-**

Table 44 - EXP Connector "JX1" Pin-out

Virtex-5 Pin#	Net Name	EXP Connector Pin # (JX2)		Net Name	Virtex-5 Pin#
V32	EXP2_SE_IO_0	2	1	EXP2_SE_IO_1	AD32
V34	EXP2_SE_IO_2	4	3	EXP2_SE_IO_3	AE34
-	**2.5V**	6	5	**2.5V**	-
V33	EXP2_SE_IO_4	8	7	EXP2_SE_IO_5	AE33
W34	EXP2_SE_IO_6	10	9	EXP2_SE_IO_7	AE32
-	**2.5V**	12	11	**2.5V**	-
W32	EXP2_SE_IO_8	14	13	EXP2_SE_IO_9	AF34
Y34	EXP2_SE_IO_10	16	15	EXP2_SE_IO_11	AF33
-	**2.5V**	18	17	**2.5V**	-
Y33	EXP2_SE_IO_12	20	19	EXP2_SE_IO_13	AG33
Y32	EXP2_SE_IO_14	22	21	EXP2_SE_IO_15	AG32
-	**2.5V**	24	23	**2.5V**	-
AA34	EXP2_SE_IO_16	26	25	EXP2_SE_IO_17	AH34
AA33	EXP2_SE_IO_18	28	27	EXP2_SE_IO_19	AH33
-	**2.5V**	30	29	**2.5V**	-
AB32	EXP2_SE_IO_20	32	31	EXP2_SE_IO_21	AH32
AB33	EXP2_SE_IO_22	34	33	EXP2_SE_IO_23	AJ34
-	**2.5V**	36	35	**2.5V**	-
AC32	EXP2_SE_IO_24	38	37	EXP2_SE_IO_25	AK33
AC34	EXP2_SE_IO_26	40	39	EXP2_SE_IO_27	AK34
AH15	EXP2_DIFF_CLK_IN_p	42	41	EXP2_SE_IO_28	AK32
AG15	EXP2_DIFF_CLK_IN_n	44	43	EXP2_SE_CLK_IN	AG21
-	**GND**	46	45	**GND**	-
AD34	EXP2_SE_IO_30	48	47	EXP2_SE_IO_29	AM33
AC33	EXP2_SE_IO_31	50	49	EXP2_SE_CLK_OUT	AJ32
-	**GND**	52	51	**GND**	-
AG10	EXP2_DIFF_p20	54	53	EXP2_DIFF_p21	AN14
AG11	EXP2_DIFF_n20	56	55	EXP2_DIFF_n21	AP14
-	**GND**	58	57	**GND**	-
AF11	EXP2_DIFF_p18	60	59	EXP2_SE_IO_32	AL34
AE11	EXP2_DIFF_n18	62	61	EXP2_SE_IO_33	AL33
-	**GND**	64	63	**GND**	-
AG8	EXP2_DIFF_p16	66	65	EXP2_DIFF_p19	AN13
AH8	EXP2_DIFF_n16	68	67	EXP2_DIFF_n19	AM13
-	**GND**	70	69	**GND**	-
AJ7	EXP2_DIFF_CLK_OUT_p	72	71	EXP2_DIFF_p17	AP12
AJ6	EXP2_DIFF_CLK_OUT_n	74	73	EXP2_DIFF_n17	AN12
-	**GND**	76	75	**GND**	-
AF8	EXP2_DIFF_p14	78	77	EXP2_DIFF_p15	AM12
AE9	EXP2_DIFF_n14	80	79	EXP2_DIFF_n15	AM11
AE8	EXP2_DIFF_p12	82	81	EXP2_DIFF_p13	AL11
AD9	EXP2_DIFF_n12	84	83	EXP2_DIFF_n13	AL10
-	**3.3V**	86	85	**3.3V**	-
AD10	EXP2_RCLK_DIFF_p10	88	87	EXP2_DIFF_p11	AK11
AD11	EXP2_RCLK_DIFF_n10	90	89	EXP2_DIFF_n11	AJ11
-	**3.3V**	92	91	**3.3V**	**-**
AC8	EXP2_DIFF_p8	94	93	EXP2_DIFF_p9	AK8
AB8	EXP2_DIFF_n8	96	95	EXP2_DIFF_n9	AK9
-	**3.3V**	98	97	**3.3V**	**-**
AA5	EXP2_DIFF_p6	100	99	EXP2_DIFF_p7	AJ9
AB5	EXP2_DIFF_n6	102	101	EXP2_DIFF_n7	AJ10
-	**3.3V**	104	103	**3.3V**	**-**
AB6	EXP2_DIFF_p4	106	105	EXP2_DIFF_p5	AH9
AB7	EXP2_DIFF_n4	108	107	EXP2_DIFF_n5	AH10
-	**3.3V**	110	109	**3.3V**	**-**
AA8	EXP2_DIFF_p2	112	111	EXP2_DIFF_p3	AF9
AA9	EXP2_DIFF_n2	114	113	EXP2_DIFF_n3	AF10
-	**3.3V**	116	115	**3.3V**	**-**
AB10	EXP2_DIFF_p0	118	117	EXP2_DIFF_p1	AC10
AA10	EXP2_DIFF_n0	120	119	EXP2_DIFF_n1	AC9
-	**GND**	122	121	**GND**	**-**
-	**GND**	124	123	**GND**	**-**
-	**GND**	126	125	**GND**	**-**
-	**GND**	128	127	**GND**	**-**
-	**GND**	130	129	**GND**	**-**
-	**GND**	132	131	**GND**	**-**

Table 45 - EXP Connector "JX2" Pin-out

3.0 Test Designs

This section describes the PCI Express example design that is pre-programmed into the P30 Flash device as well as the test files provided on the Design Resource Center (DRC) web site: www.em.avnet.com/drc. These test files are used to verify some of the functionality of the board and may require additional test apparatus. The remaining production tests are not included with the kit because they require custom-designed test fixtures.

If the Flash device has been erased, the MCS file containing the test designs is available on the Design Resource Center web site: www.em.avnet.com/drc. The Flash can be re-programmed by using the Xilinx iMPACT software. In Boundary-Scan mode, initialize the JTAG chain and select the "Enable Programming of BPI Flash Device Attached to this FPGA". You may have to assign a dummy bit file in order to proceed. Next, assign the MCS file to the Flash device in the "Add PROM File" window and then select the Flash part number: "INTEL28F**128**P30" for the LX50T/SX50T FPGA or "INTEL28F**256**P30" for the LX110T/SX95T FPGA. Last, right-click on the Flash device and select "Program" and then "Erase before Programming" to program the Flash. The "Verify" option is not supported by the Virtex-5 LXT/SXT PCI Express board and should not be used. After iMPACT indicates the programming was successful (this will take several mintues), verify the jumper labeled "JP1" on the board is set for "BPI" mode (jumper installed across JP1 pins 1-2) to put the FPGA in Master BPI-Up mode and then cycle power to configure the FPGA with file programmed into the Flash.

The Ethernet and Factory test designs available on the DRC web site use a terminal session as the user interface. Using a straight-through serial cable, connect the Virtex-5 LXT/SXT PCI Express Board to a PC. Open a terminal session and configure it for 19200 baud, 8 data bits, no parity, 1 stop bit and no flow control (19200-8-N-1-N).

3.1 PCI Express PIO Example

The PCI Express Programmed Input Output (PIO) Example design is generated by the CORE Generator tool supplied with the Xilinx ISE software. The source code for the PIO Example is one of the deliverables provided by CORE Generator after customizing the Xilinx PCI Express Endpoint LogiCore. The design implements an 8192 byte Memory Mapped I/O space in the Virtex-5 BlockRAM, behind the PCI Express Endpoint core. This 32-bit MMIO space is accessible through Memory Read 32 and Memory Write 32 TLPs. The PIO reference design generates a Completion with 1 DWORD of payload in response to a valid Memory Read 32 TLP request presented to it by the PCI Express Endpoint core. The PIO design also processes a Memory Write 32 with 1 DWORD payload, by updating the payload into the target address in the Virtex-5 BlockRAM space.

Using the default jumpers (as shipped), the PIO design will boot from the Flash when power is applied to the board. Before plugging the board into a PCI Express slot, verify the fuse is installed in the fuse socket labeled "F1" and that the power switch labeled "SW1" is in the "ON" position. The Virtex-5 LXT/SXT PCI Express board will fit in either a x8 or x16 PCI Express motherboard slot (host connector). PCI Express host connectors do not support down-plugging so the Virtex-5 board will NOT fit in slots smaller than x8 (do not attempt to use the board in a x1 or x4 slot). Once the PC boots, the blue "DONE" LED should illuminate as well as a few in the bank of eight user LEDs (D1 through D8). A graphical Windows tool like PCItree can be used to read-back the configuration space implemented in the Virtex-5 FPGA and perform memory transactions to the 8KB of BlockRAM memory mapped to BAR0. A shareware version of PCItree can be downloaded from the PCItree web site (www.pcitree.de).

3.2 Ethernet Test

The Ethernet Test design provides the user with the ability to ping the Virtex-5 LXT/SXT PCI Express board to verify network connectivity via the on-board National 10/100/1000 Mbps Ethernet PHY. The National PHY supports auto-MDIX mode, which allows either a straight-through or a cross-over Ethernet cable to be used. The default IP address of the board is 172.16.158.147. To ping the board, plug an Ethernet cable into the RJ45 connector labeled "J9". Then change the IP address of the board to match the subnet of the PC or network it's connected to using a terminal program configured as shown in Section 3.0 (19200-8-N-1-N). At the prompt, type 'i' and then enter the new IP address for the board (first three fields must match the IP address of the PC: MMM.MMM.MMM.xxx; the last field must be different). Use periods '.' between fields and hit the <enter> key when finished. Then open a command shell on the PC (Start Menu -> Run, cmd) and type 'ping MMM.MMM.MMM.xxx'. You should see four replies to the ping request.

3.3 Factory Test

The Factory Test verifies the electrical connectivity of the DDR2 SDRAM and Flash memory, the user LEDs and switches, and the EXP expansion connectors (requires a Samtec loopback cable). The user can initiate the tests by typing 'test <enter>' in a terminal session configured as shown in Section 3.0 (19200-8-N-1-N). Some of the tests require user inputs and observation (watching the LEDs and pressing the switches). The cumulative results are displayed at the completion of test processes. The EXP loopback test requires a Samtec cable, part number: EQCD-060-12.00-SED-SEU-1 or similar. Check the following catalog page for more information: http://www.samtec.com/ftppub/pdf/EQCD.PDF.

4.0 Revisions

V1.0	Initial release for production board (AES-XLX-V5-PCIe-PCB-B)	November 26, 2007

Appendix A

This section provides a description of the jumper settings for the Virtex-5 LXT/SXT PCI Express board. The board is ready to use out of the box with the default jumper settings. The following figure depicts a map of the component side of the board with Jumper/Header/Connector locations detailed. The jumper sites are colored pink below.

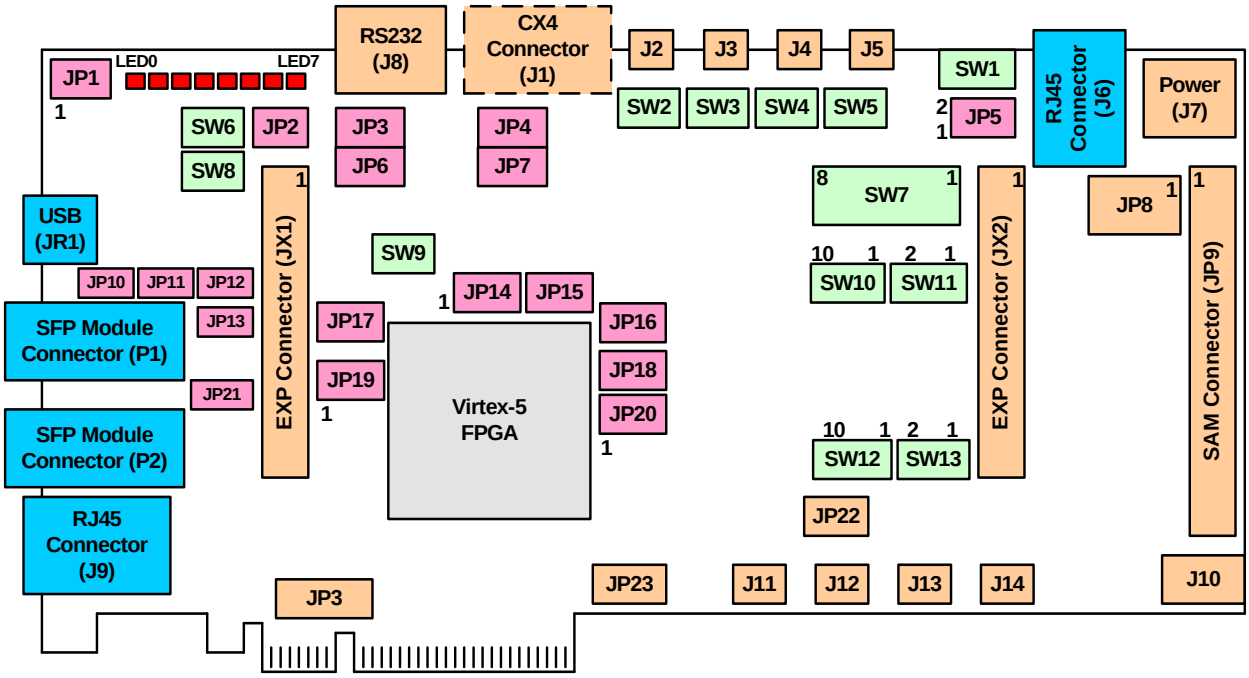


Figure 25 - Board Jumpers/Headers/etc.

JP1 "Configuration mode selection" – Use to select the configuration mode for the FPGA. Installing a jumper across pins 1-2 on JP1 will set the FPGA mode pins for BPI-Up mode, causing the FPGA to load from the Flash device. Installing a jumper across pins 2-3 sets the configuration mode to Boundary-Scan (JTAG). Default: JP1 1-2 (BPI) as shown in Figure 25. See section 2.2.3 for more information.

Config Mode	M2	M1	M0
BPI-Up	0	1	0
Boundary Scan	1	0	1

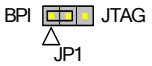


Figure 26 - Configuration Mode Jumper

JP2 "USB DIS" – USB Disable, install a shunt to hold the Cypress EZ-USB device in reset. When open, the USB reset line is controlled by either an I/O pin of the FPGA or the push-button labeled "SW8". Default: Open, the FPGA or push-button controls the USB reset.

JP3 "R1IN" – Connects the "R1IN" signal of the RS232 transceiver to either pin 2 or pin 3 of the DB9 connector. Install a shunt across pins 1-2 for DTE mode or pins 2-3 for DCE mode. Default: JP3 2-3.

JP4 "R2IN" – Install a shunt to connect the second RX port of the RS232 transceiver to the DB9 connector for hardware handshaking. This can be used to implement the ready to send (RTS) signal. Default: Open.

JP5 "PCIe Lane Width" – Selects the number of PCI Express lanes to advertise to the host PC. A single jumper is installed to connect the PRSNT1# pin to the PRSNT2# pin that corresponds to the desired lane width (x1, x4 or x8). This allows the user to force fewer lanes to be used to target applications requiring less than 8 lanes. Default: JP5 5-6 (8 lanes).

JP6 “T1OUT” – Connects the “T1OUT” signal of the RS232 transceiver to either pin 2 or pin 3 of the DB9 connector. Install a shunt across pins 1-2 for DCE mode or pins 2-3 for DTE mode. Default: JP6 1-2.

JP7 “T2OUT” – Install a shunt to connect the second TX port of the RS232 transceiver to the DB9 connector for hardware handshaking. This can be used to implement the clear to send (CTS) signal. Default: Open.

JP8 “PC4/USB JTAG” – Ribbon cable connector used by the Xilinx Parallel Cable IV and Platform Cable USB.

JP10 – USB Serial EEPROM write protect, install a shunt to protect programmed data. Default: Open, read/write enabled.

JP11 – Test access to the 8051 serial port of the Cypress FX2 device.

JP12 – USB Serial EEPROM address select, Default: Open.

JP13 “P1 EN” – SFP0 Enable, install a shunt to enable a module plugged into the Small Form Pluggable (SFP) cage labeled “P1” on the board. Default: Open (disabled).

JP14 “FLSH WP” – Flash Write-protect Enable, install a shunt to protect programmed data in the Flash memory. Default: JP14 1:2, read/write enabled (unprotected).

JP15 – Test access to the DXP and DXN pins of the FPGA.

JP16 “VIO1 SE” – Vcco selectable voltage for Bank 11 on the Virtex-5 LXT/SXT PCI Express Board. This selects the voltage level for the single-ended signal group on the EXP connector labeled “JX1”. The following figure shows JP16 in its default configuration (VIO_EXP1_SE = +2.5V).

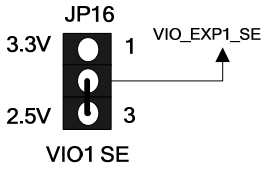


Figure 27 - VIO1 SE "JP16"

JP17 “HSWAP” – Enables pull-ups on the Virtex-5 I/O pins during configuration. Install a jumper to enable the configuration pull-ups. Default: Open; pull-ups disabled.

JP18 “VIO2 SE” – Vcco selectable voltage for Bank 13 on the Virtex-5 LXT/SXT PCI Express Board. This selects the voltage level for the single-ended signal group on the EXP connector labeled “JX2”. The following figure shows JP18 in its default configuration (VIO_EXP2_SE = +2.5V).

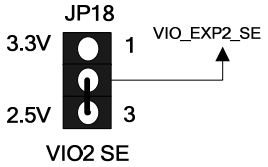


Figure 28 – VIO2 SE "JP18"

JP19 “VIO1 DP” – Vcco selectable voltage for Banks 3, 12 and 20 on the Virtex-5 LXT/SXT PCI Express Board. This selects the voltage level for the differential signal group on the EXP connector labeled “JX1”. The following figure shows JP19 in its default configuration (VIO_EXP1_DP = +2.5V).

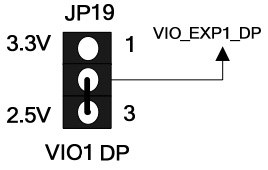


Figure 29 - VIO1 DP "JP19"

JP20 “VIO2 DP” – Vcco selectable voltage for Banks 4, 18 and 22 on the Virtex-5 LXT/SXT PCI Express Board. This selects the voltage level for the differential signal group on the EXP connector labeled “JX2”. The following figure shows JP20 in its default configuration (VIO_EXP2_DP = +2.5V).

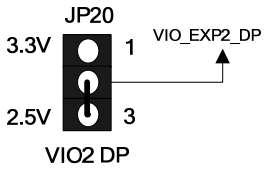


Figure 30 – VIO2 DP "JP20"

JP21 “P2 EN” – SFP1 Enable, install a shunt to enable a module plugged into the Small Form Pluggable (SFP) cage labeled “P2” on the board. Default: Open (disabled).

JP22 “FAN” – +5V Active Heat sink power.

JP23 – +12V Active Heat sink power.