KIP Heidelberg

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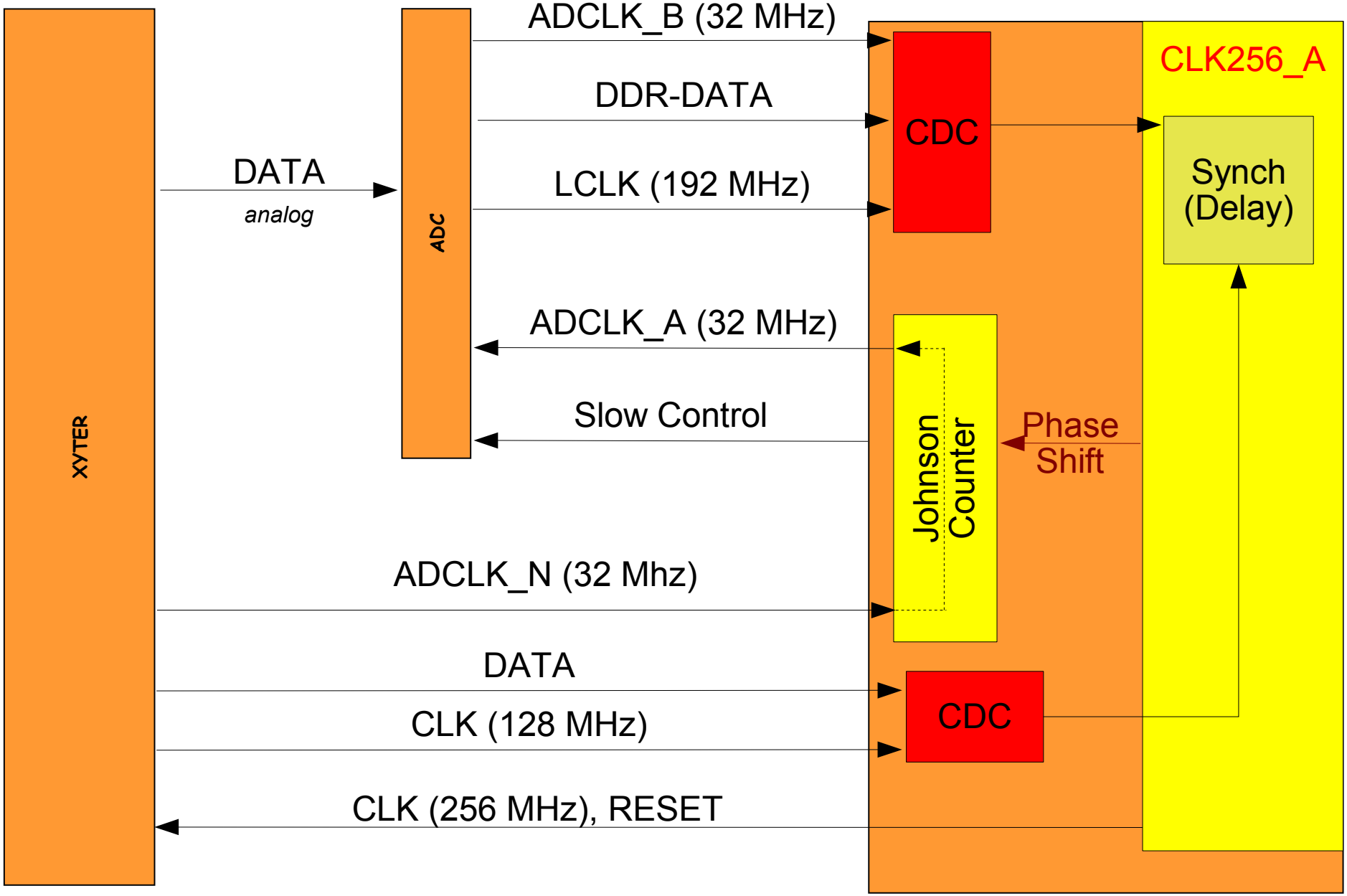
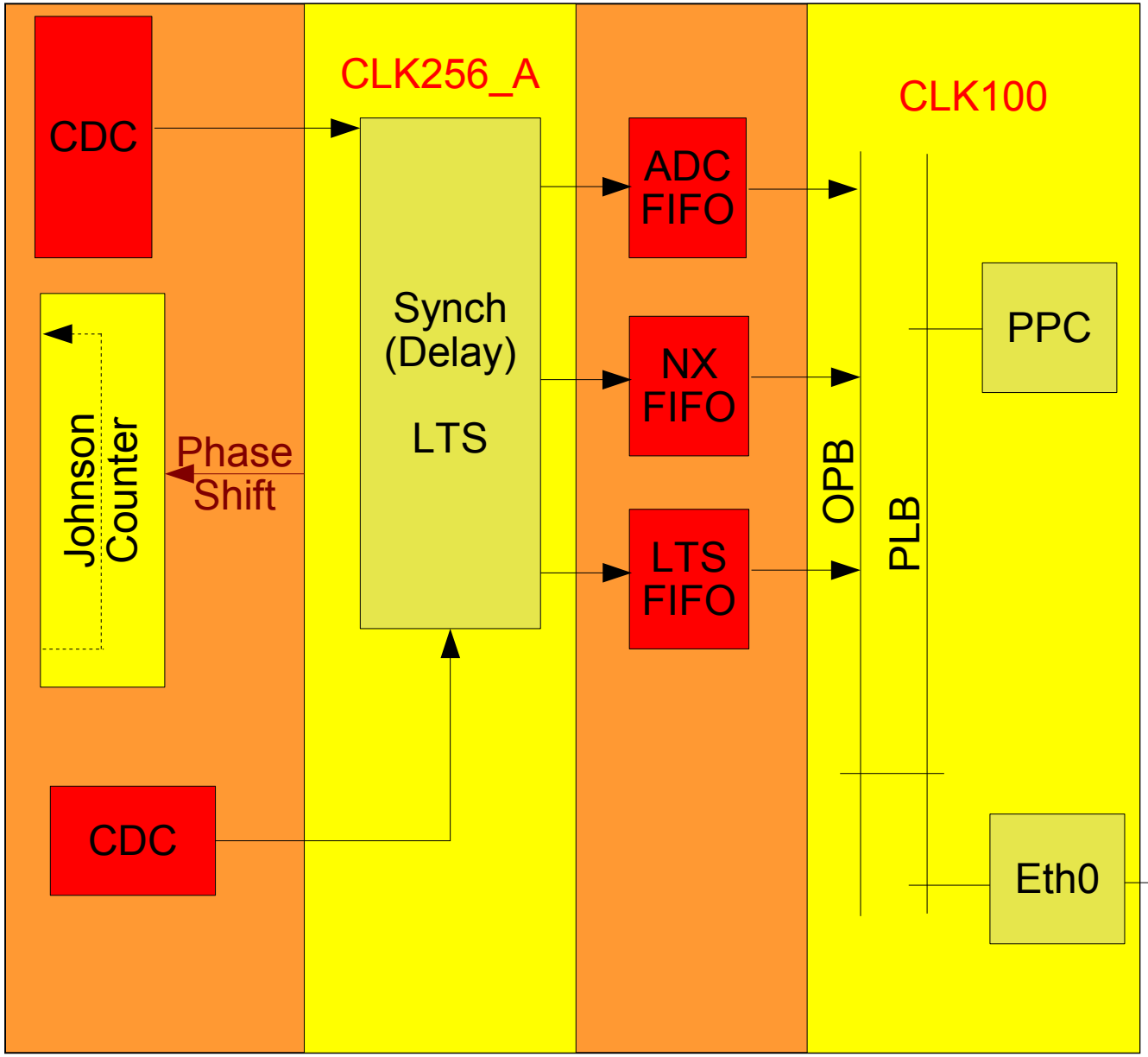
Status of the ROC firmware

Overview


XYTER
DATA
analog
ADC
ADCLK_B (32 MHz)
DDR-DATA
LCLK (192 MHz)
ADCLK_A (32 MHz)
Slow Control
ADCLK_N (32 Mhz)
DATA
CLK (128 MHz)
CLK (256 MHz), RESET
CDC
CDC
CLK256_A
Synch
(Delay)
Johnson
Counter
Phase
Shift

SysCore in Detail



Two Delays:

1. ADC-NX-Delay
2. NX-ROC-Delay

Auto Calibration for ADC-NX-Delay

- The Latency is settable via OPB
- It determines the delay between ADC and NX in 32MHz-Clock-Cycles

- The Johnson-Counter and the BUFG are also settable via OPB
- They are used to calibrate the ADC-Input-Clock

- Autodelay:

  test latency from 5 to 7:
    test BUFG from 0 to 1:
      test Johnson-Counter-Shift from 0 to 15:
        send 500 pulses and measure the ADC values

  - use the latency, BUFG and shift with the highest average ADC value

```
SysCore> auto

500 --- 5, 0, 0 --- avg: 8B2
500 --- 5, 1, 0 --- avg: 887
500 --- 5, 2, 0 --- avg: 870
500 --- 5, 3, 0 --- avg: 843
500 --- 5, 4, 0 --- avg: 829
500 --- 5, 5, 0 --- avg: 80C
500 --- 5, 6, 0 --- avg: 804
500 --- 5, 7, 0 --- avg: 7FE
500 --- 5, 8, 0 --- avg: 7FF

...
```

Auto Calibration for ADC-NX-Delay


```
SysCore> auto

..
500 --- 5, 14, 1 --- avg: 7FD
500 --- 5, 15, 1 --- avg: 891
500 --- 6, 0, 0 --- avg: 88E
500 --- 6, 1, 0 --- avg: 894
500 --- 6, 2, 0 --- avg: 899
500 --- 6, 3, 0 --- avg: 8A0
500 --- 6, 4, 0 --- avg: 8A5
500 --- 6, 5, 0 --- avg: 8AB
500 --- 6, 6, 0 --- avg: 8B0
500 --- 6, 7, 0 --- avg: 8B2
500 --- 6, 8, 0 --- avg: 8B3
500 --- 6, 9, 0 --- avg: 8B2
500 --- 6, 10, 0 --- avg: 8B2
500 --- 6, 11, 0 --- avg: 8AE
500 --- 6, 12, 0 --- avg: 8AC
500 --- 6, 13, 0 --- avg: 8A8
500 --- 6, 14, 0 --- avg: 8A1
500 --- 6, 15, 0 --- avg: 888
500 --- 6, 0, 1 --- avg: 891
500 --- 6, 1, 1 --- avg: 896
500 --- 6, 2, 1 --- avg: 89E
500 --- 6, 3, 1 --- avg: 8A2
500 --- 6, 4, 1 --- avg: 8A9
500 --- 6, 5, 1 --- avg: 8AD
500 --- 6, 6, 1 --- avg: 8B2
500 --- 6, 7, 1 --- avg: 8B3
500 --- 6, 8, 1 --- avg: 8B3
500 --- 6, 9, 1 --- avg: 8B3
500 --- 6, 10, 1 --- avg: 8B1
500 --- 6, 11, 1 --- avg: 8AD
500 --- 6, 12, 1 --- avg: 8AA
500 --- 6, 13, 1 --- avg: 8A5
500 --- 6, 14, 1 --- avg: 899
500 --- 6, 15, 1 --- avg: 88A
500 --- 7, 0, 0 --- avg: 84B
500 --- 7, 1, 0 --- avg: 84D
..
```

Auto Calibration for ADC-NX-Delay

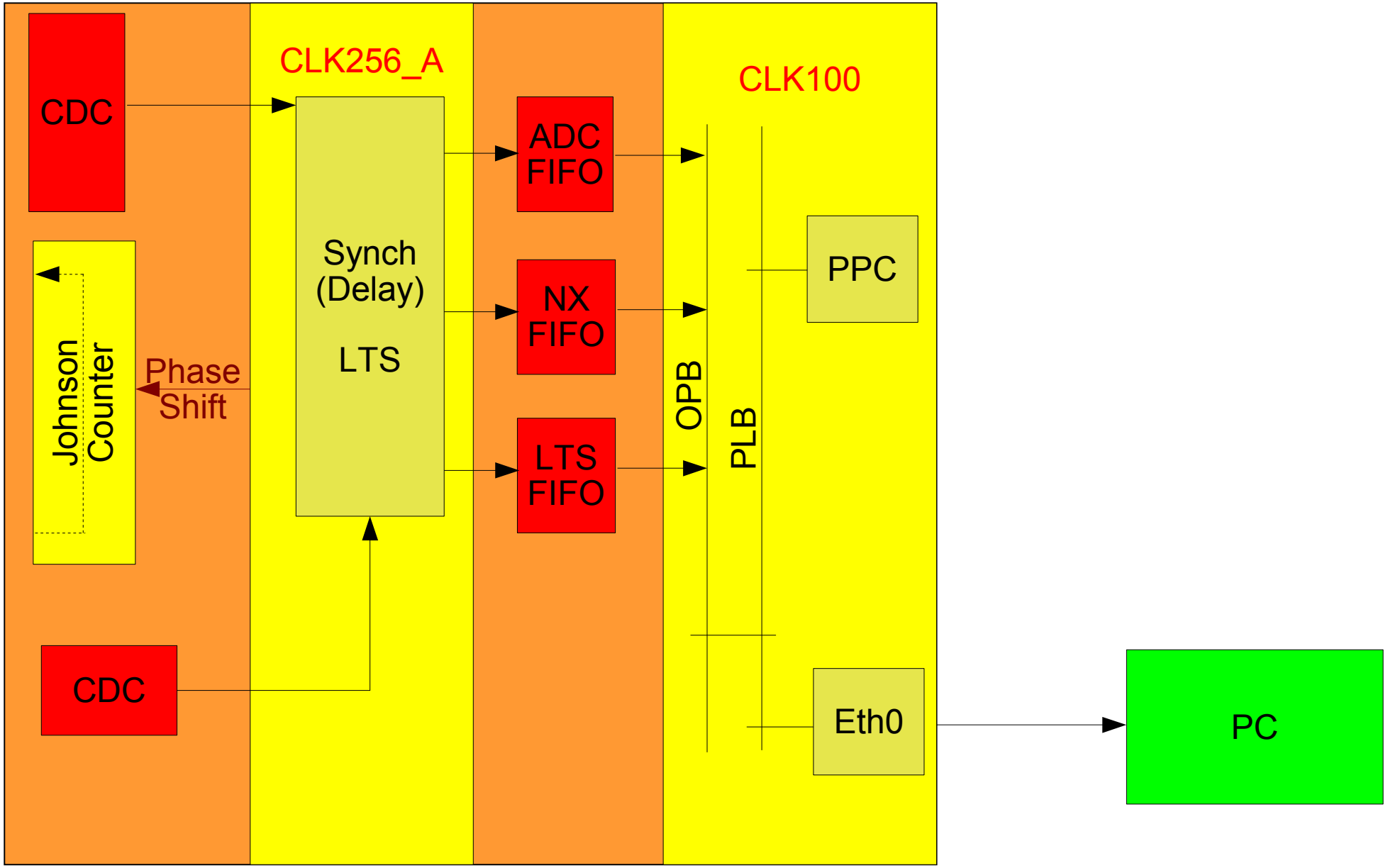

```
SysCore> auto

...

Latency: 6
sr_init: 8
bufg   : 0
max-adc: 8B3

Setting the latency to 6 ...
OK.

Using the measured shift of 16 ...
SR_INIT:     FF00
BUFG_SELECT: 0


SysCore>
```

Auto Calibration for NX-ROC-Delay

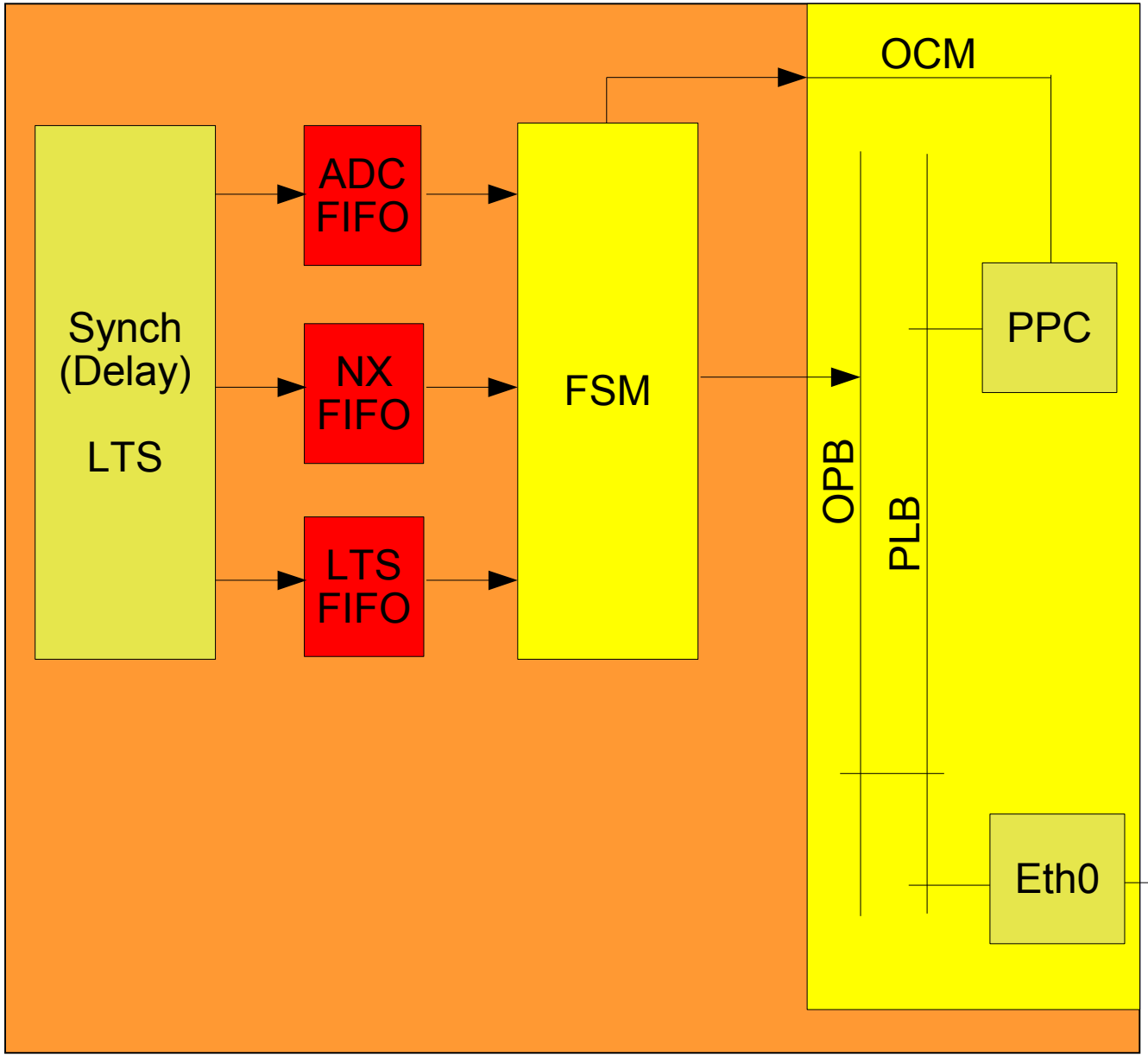
- The TS-Delay is settable via OPB
- It determines the number of 256MHz-Clock-Cycles until the LTS starts (after a Reset)
- Autodelay:
  - set delay to 0
  - reset
  - send “lonely” pulses until FIFO is full
  - determine the smallest delay
  - set delay to this delay
  - reset

```
SysCore> autodelay

Please wait for Reset...
OK.

Setting the measured TS-Delay of 18 + 1 ...
OK.
Please wait for Reset...
OK.


SysCore>
```

OCM-Burst


CDC
CLK256_A
CLK100
ADC FIFO
Synch (Delay) LTS
PPC
NX FIFO
Johnson Counter
Phase Shift
OPB
PLB
LTS FIFO
CDC
Eth0
PC

OCM-Burst



Two Modes:

Prefetch OFF:
Slow Access via OPB

Prefetch ON:
Fast Access via OCM
Debugging via OPB

Ethernet Data Format

- Message length: 48 bit
- For Burst the whole messaging is done in hardware
  (even Epoch-Markers are inserted automatically by the FSM)
- Thus: one read access reads 3 OCM-Words (à 32 bit)
  this are 2 messages
- Data rate: 50MB/s (at 100MHz PPC-Clock, limited by OCM)

- 5 Message-Types:

• NOP	000	represents an empty ROC-FIFO
• hit data	001	contains the data of one hit
• epoch marker	010	represents the epoch & missed events
• synch marker	011	t.b.d.
• system message	100	t.b.d.

Ethernet Data Format

NOP:

Type	3 bit	*= 000*
unused	45 bit	*(not valid)*

Hit Data:

Type	3 bit	*= 001*
ROC#	3 bit	
NX#	2 bit	
MSB of ROC-TS	3 bit	*(NX-FIFO fill level)*
NX-TS	14 bit	
ID	7 bit	
unused	1 bit	
ADC value	12 bit	
PileUp	1 bit	
OverF	1 bit	
last Epoch?	1 bit	

Ethernet Data Format

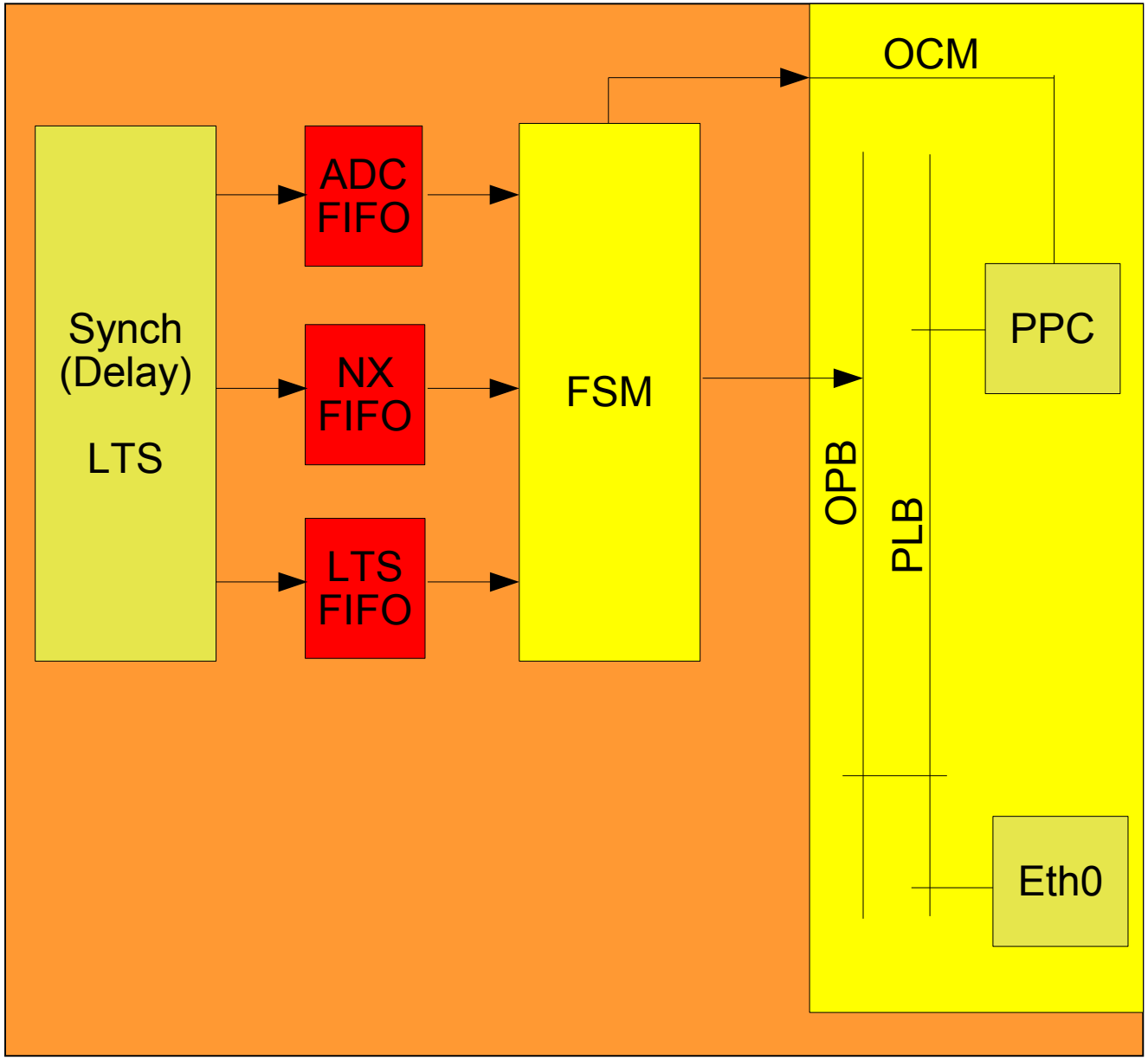
Epoch Marker:

Type	3 bit	= *010*
ROC#	3 bit	
unused	2 bit	
Epoch	32 bit	
Missed Events	8 bit	*(255 means: 255 or more)*

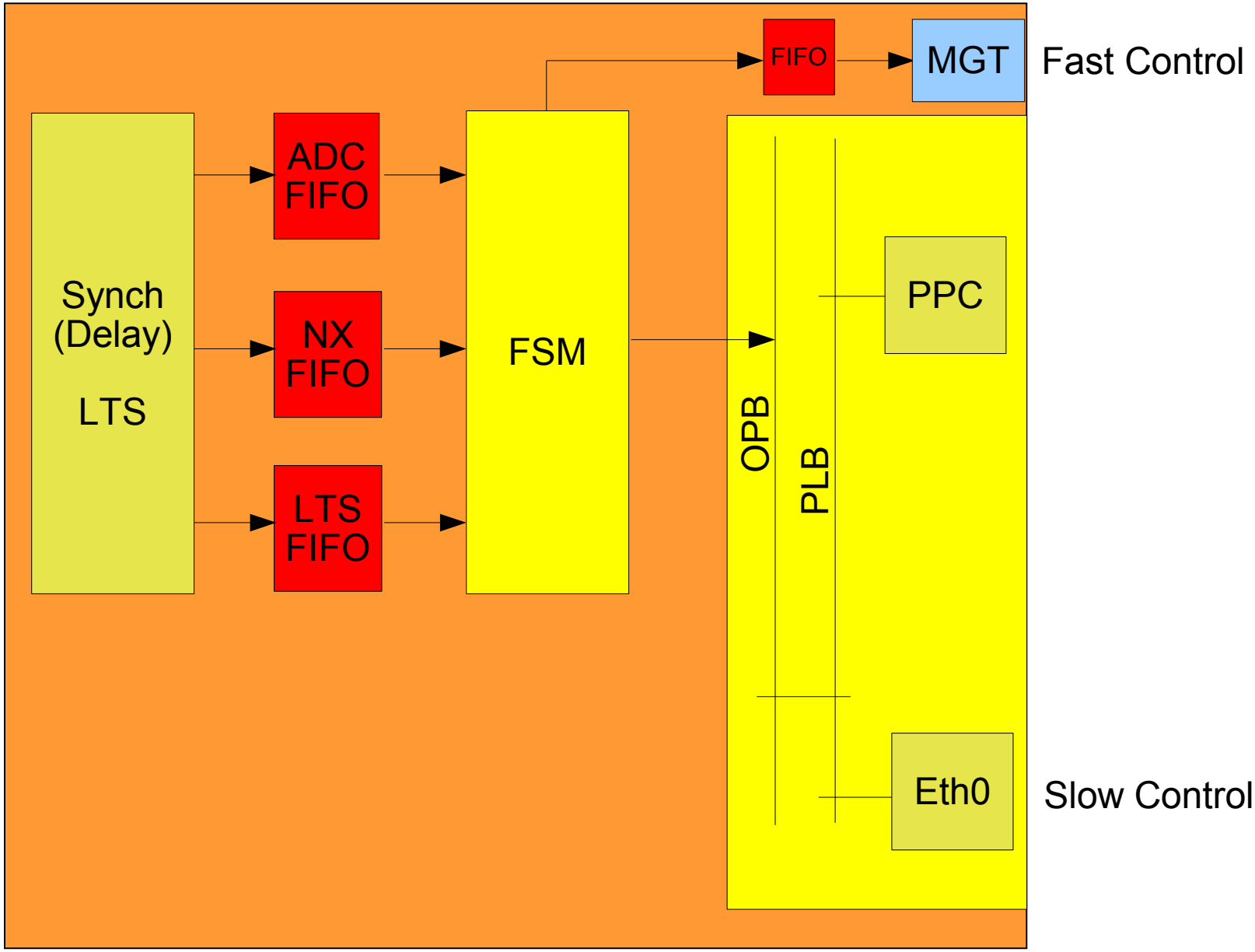
Synch Marker:

Type	*3 bit*	= *011*
t.b.d.		

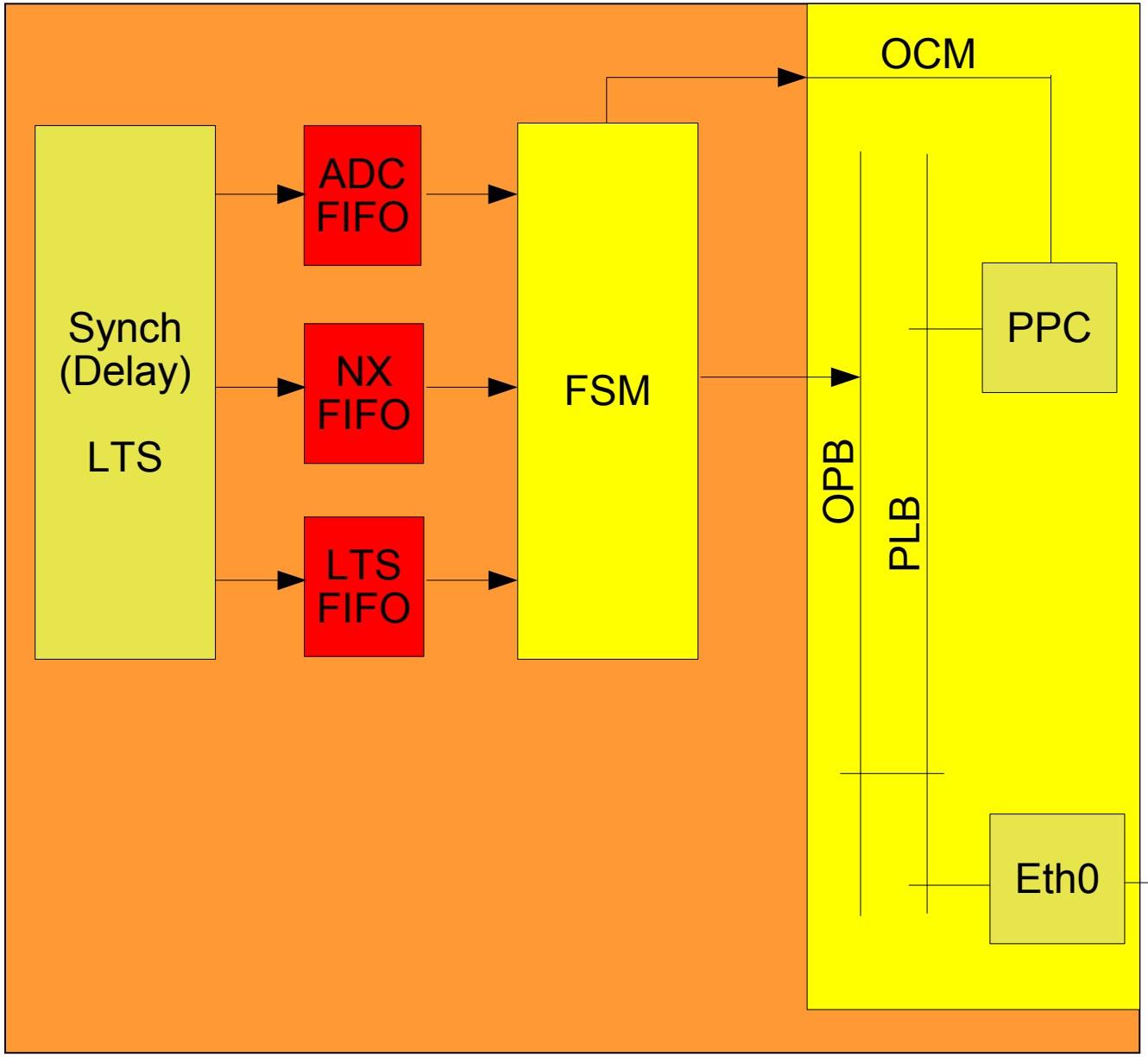
Preview


OCM
ADC FIFO
NX FIFO
LTS FIFO
Synch (Delay)
LTS
FSM
PPC
Eth0
OPB
PLB

Preview


FIFO
MGT
Fast Control
ADC FIFO
Synch (Delay)
LTS
NX FIFO
FSM
PPC
OPB
PLB
LTS FIFO
Eth0
Slow Control

Software



PPC:
Raw Ethernet:
UDP / IP
(with credits)

90 Mbit / s

2 Ports:
Slow Control
OCM-Burst

PC:
C++ - class for
network access